



Schematic Package Supplement to the Gauntlet™ Operators Manual

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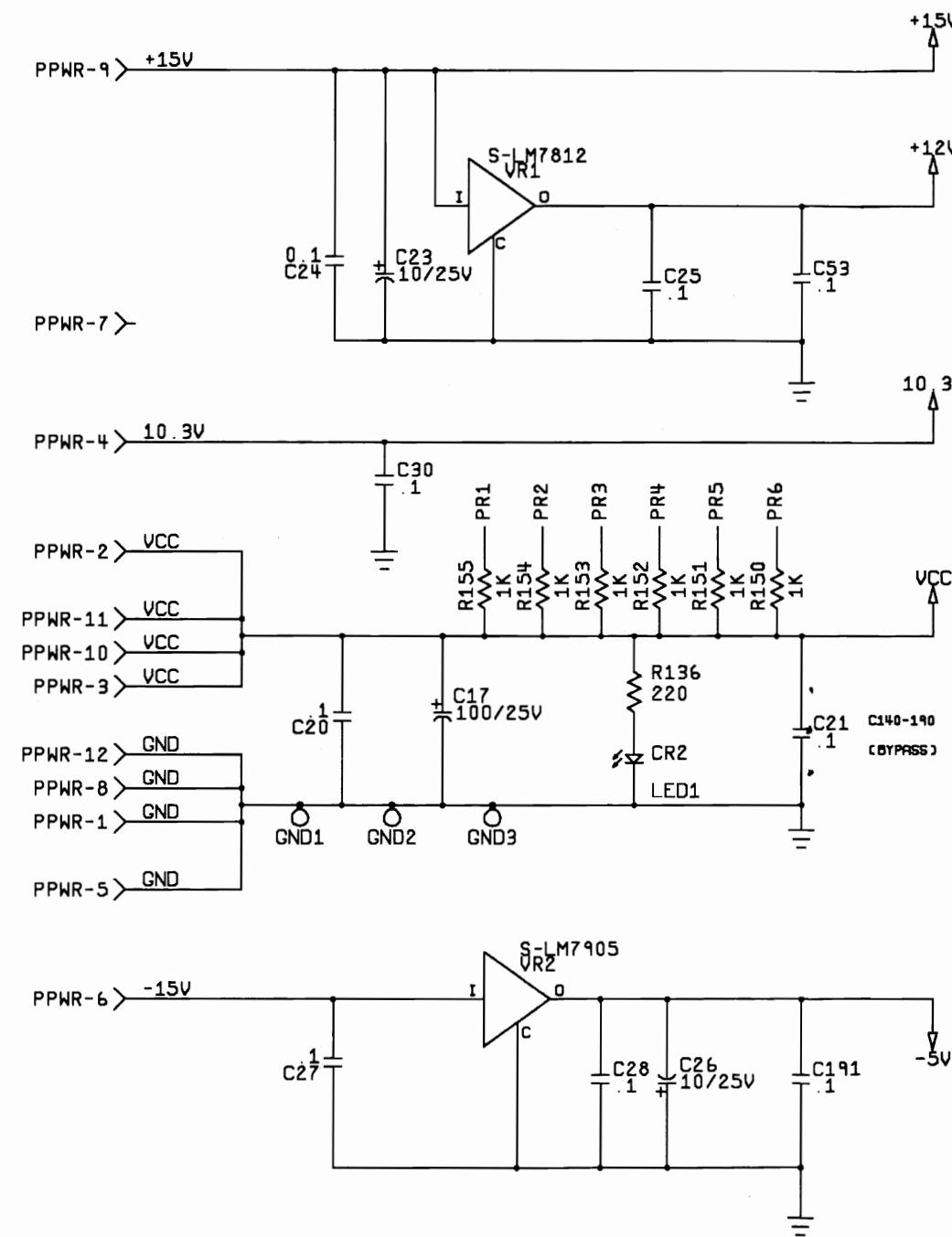
NOTE
This staple temporarily holds the schematic package together. Remove the staple before using these schematics.



NOTE

In the schematics printed on Sheets 1-16 a slash (/) in front of a signal name indicates an active low signal. In the signal name glossary (printed at the end of this schematic package) these signals are overscored, e.g., COMPSYNC.

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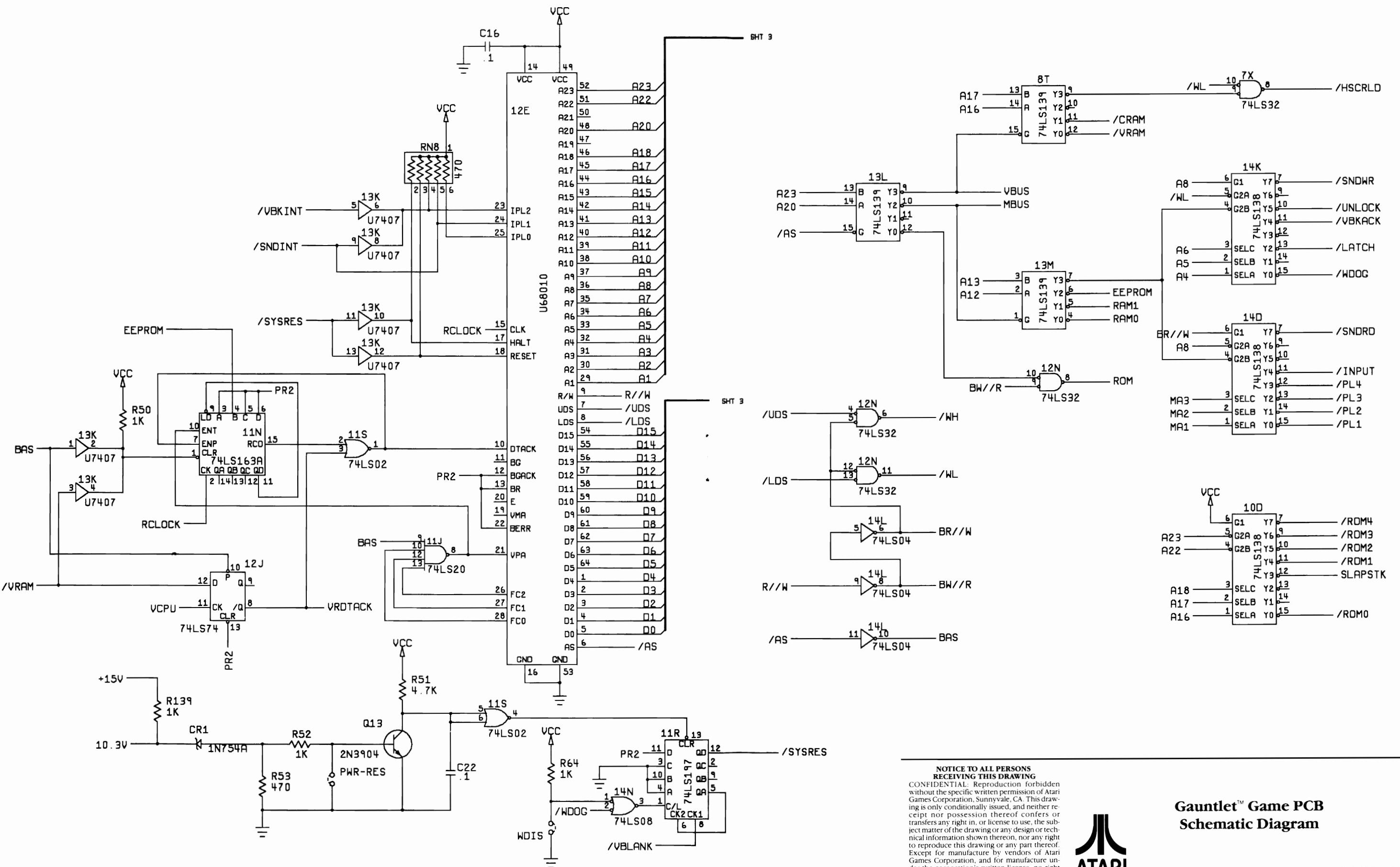


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Gauntlet™ Game PCB Schematic Diagram



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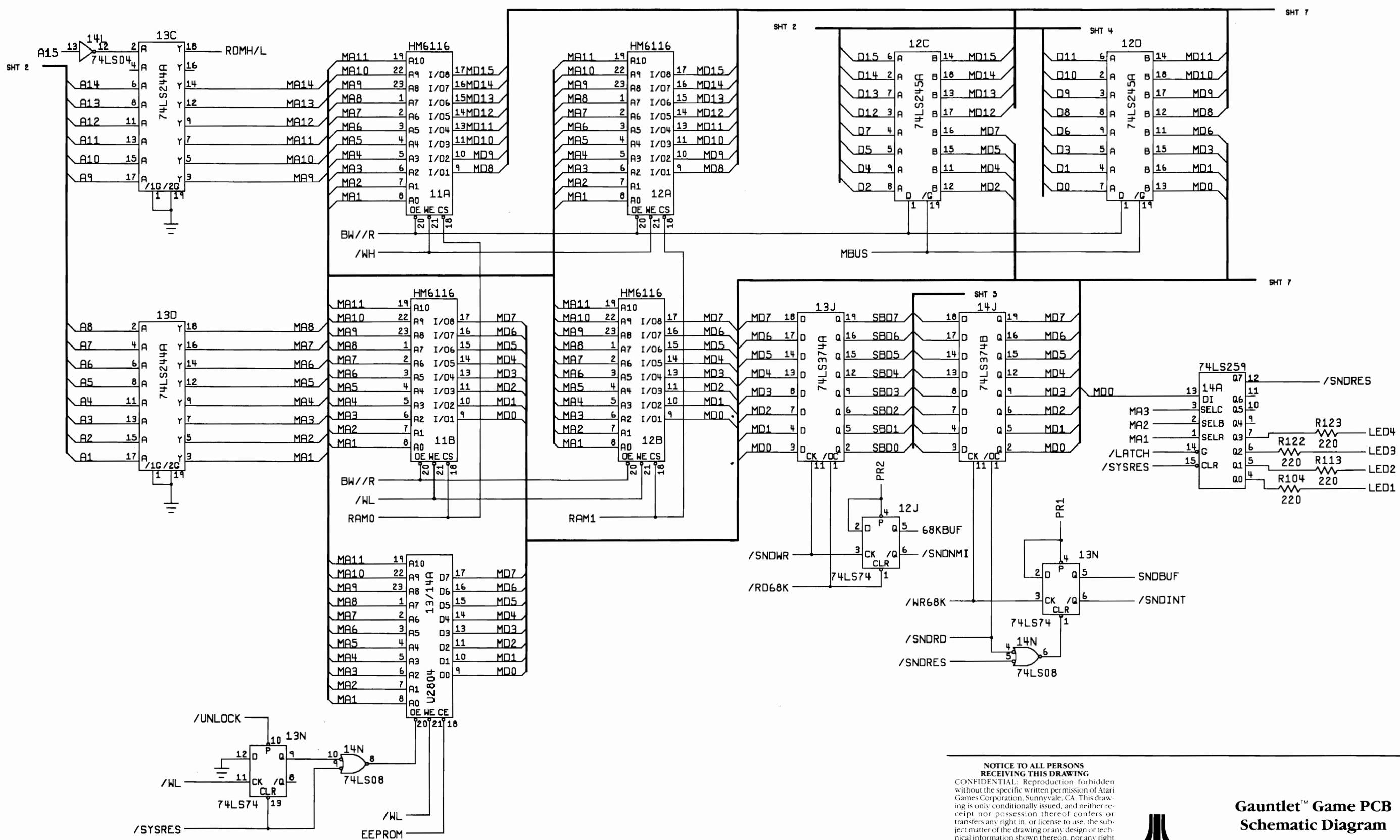


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Gauntlet™ Game PCB Schematic Diagram



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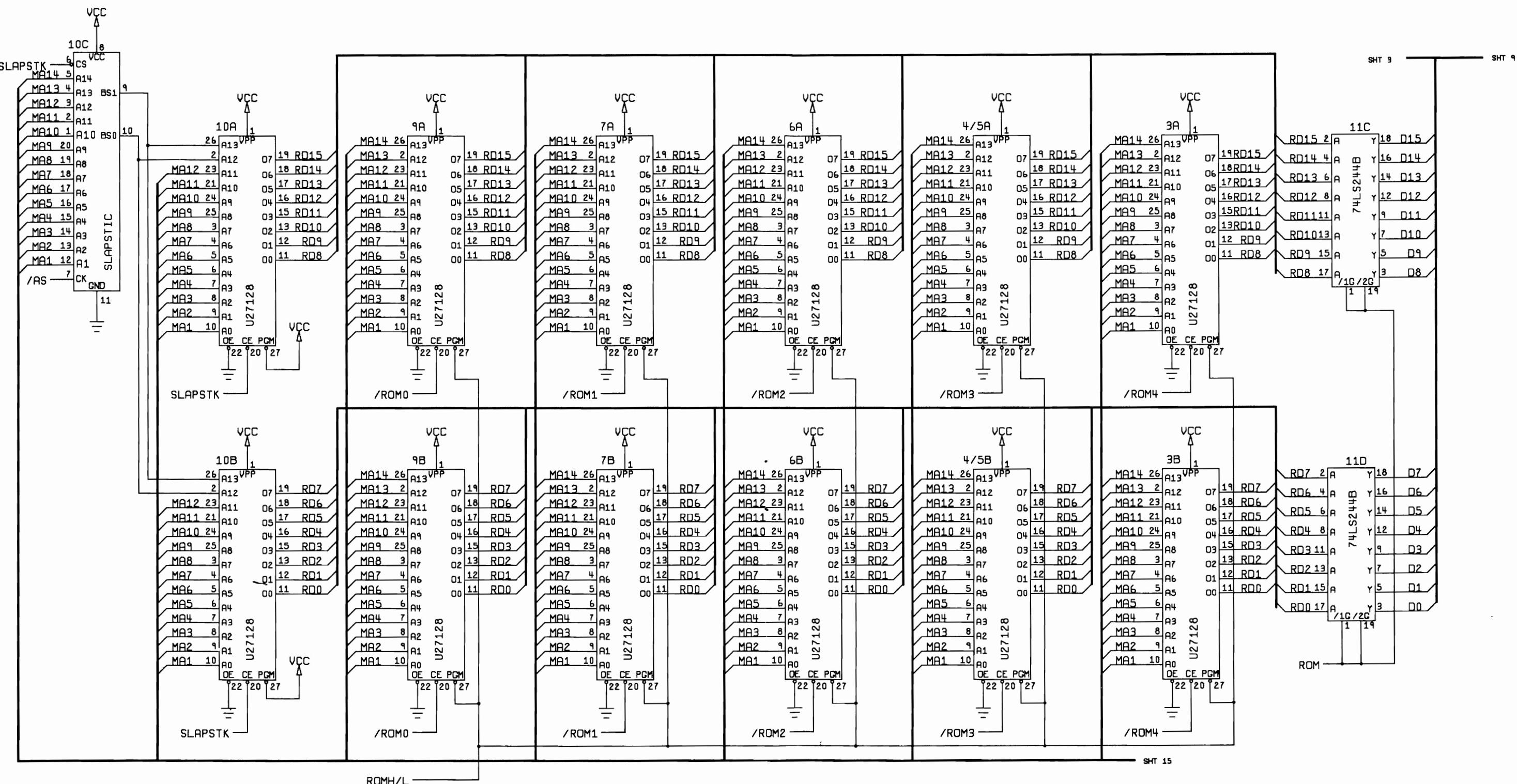


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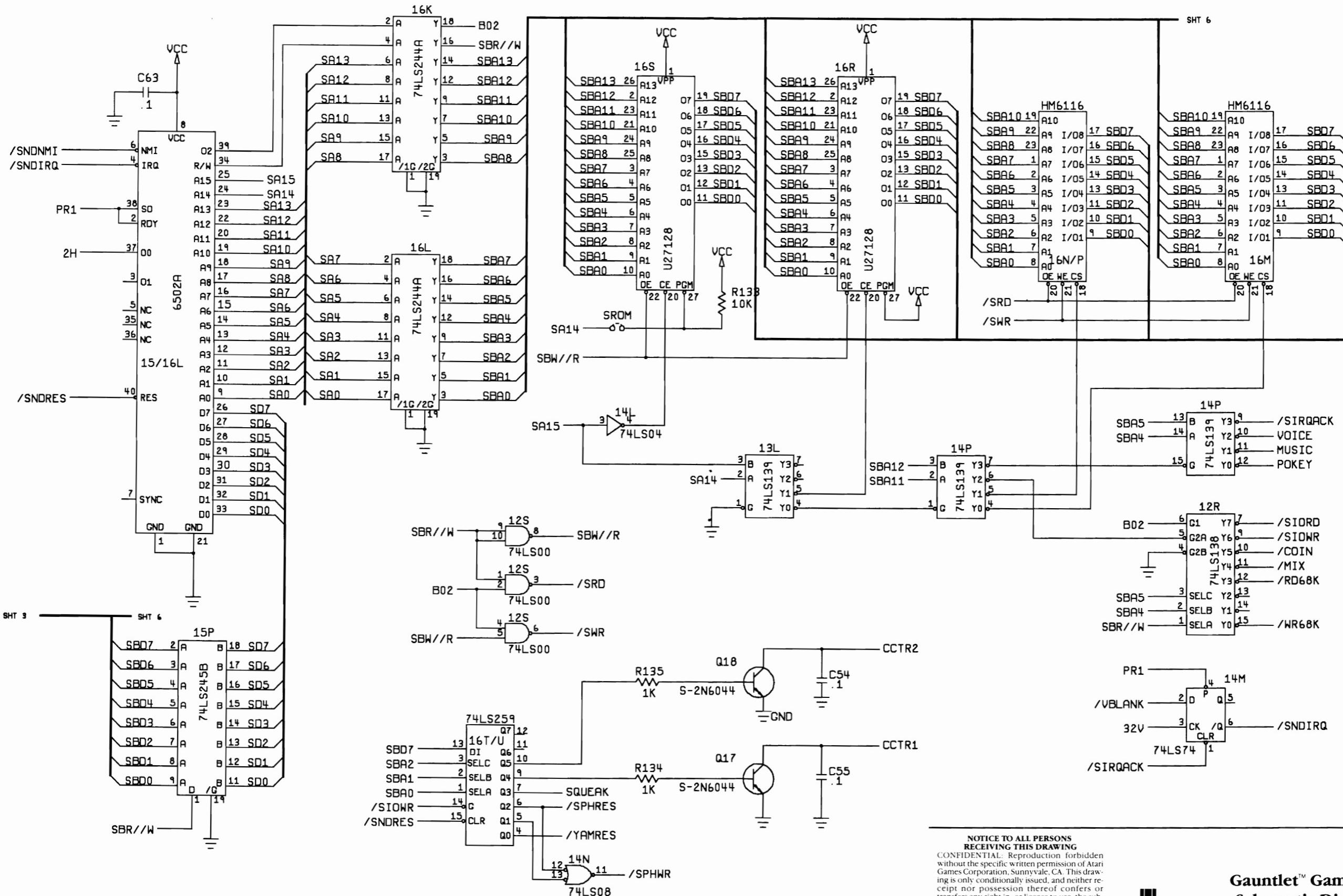


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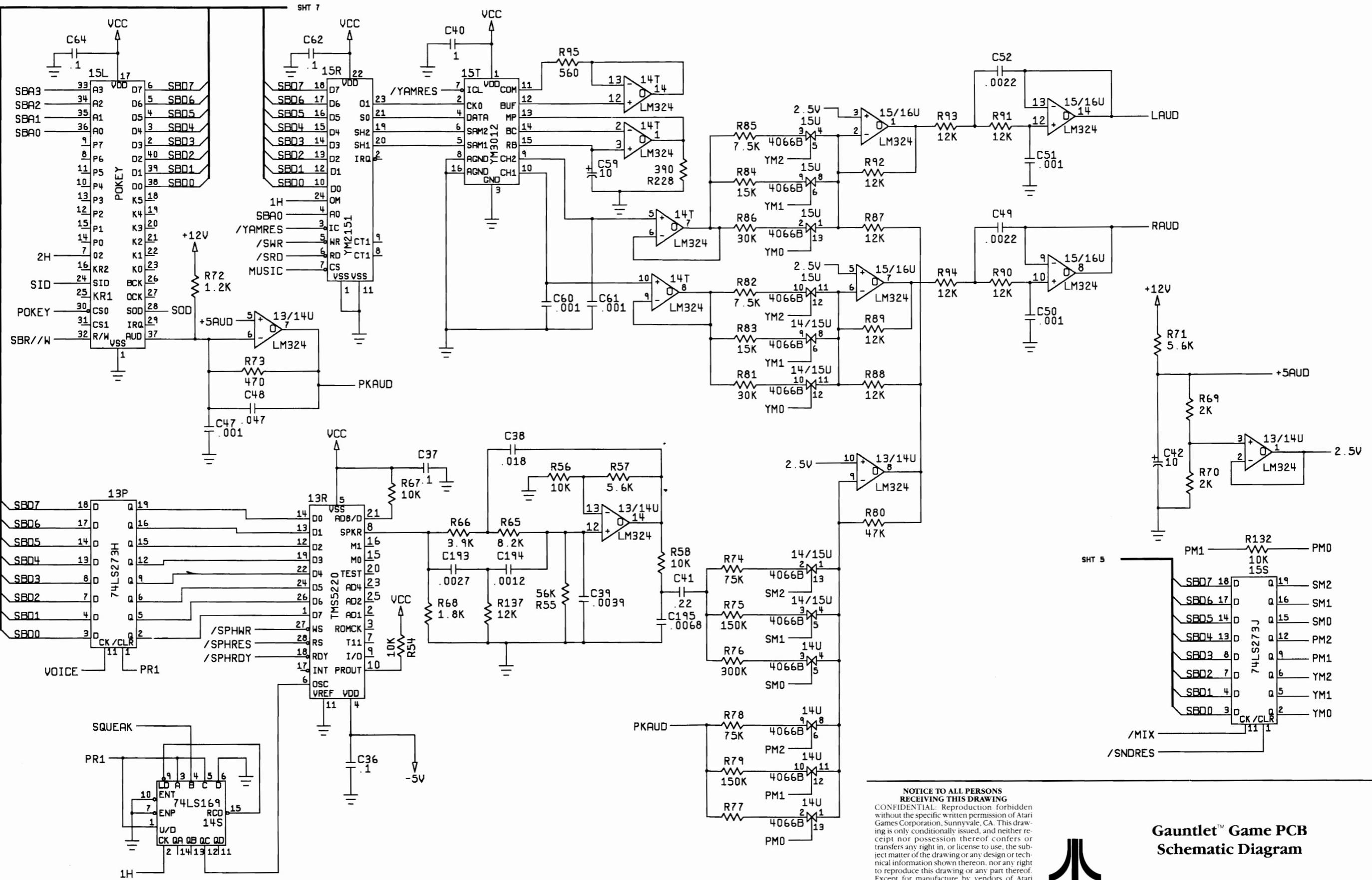
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Gauntlet™ Game PCB
Schematic Diagram

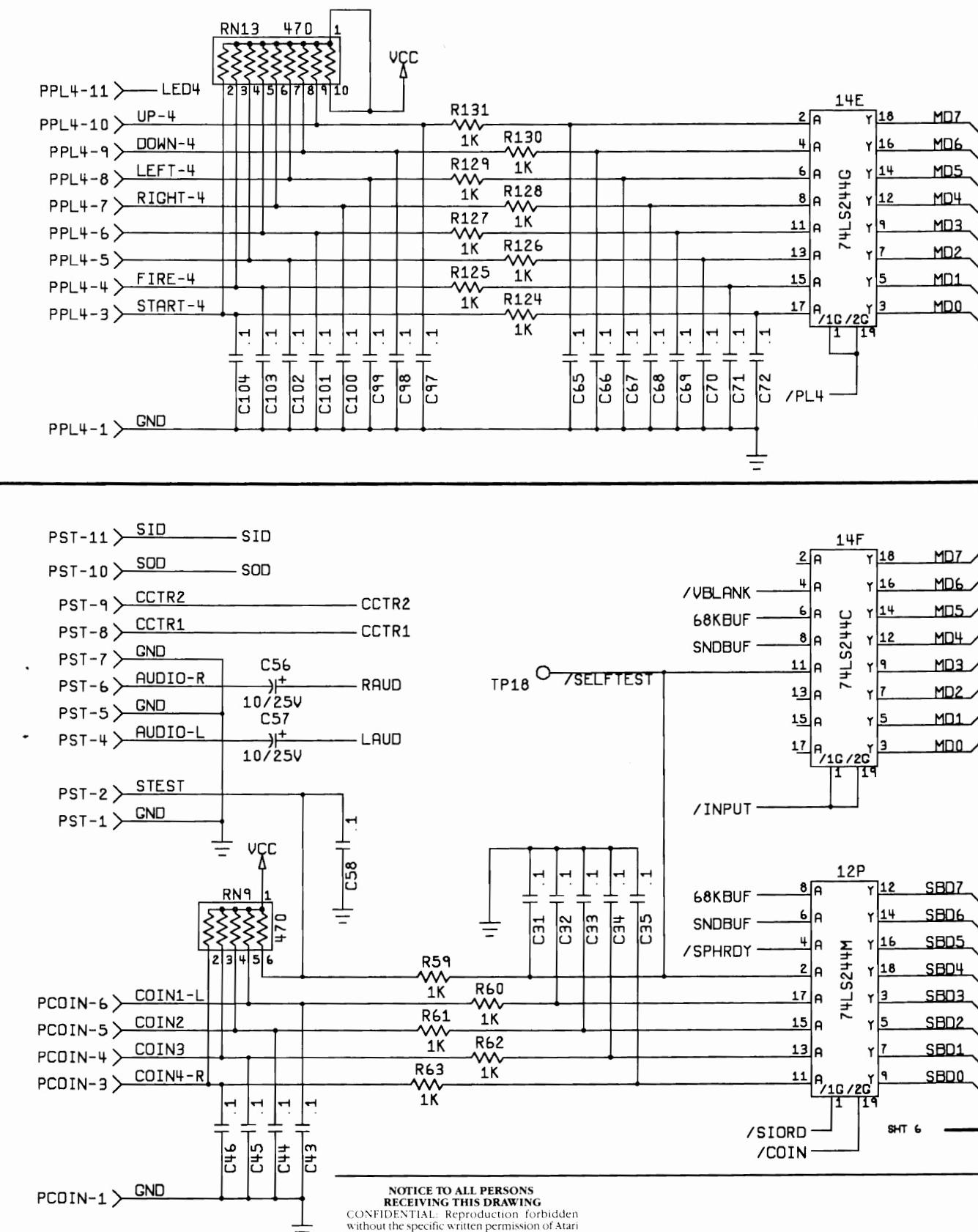
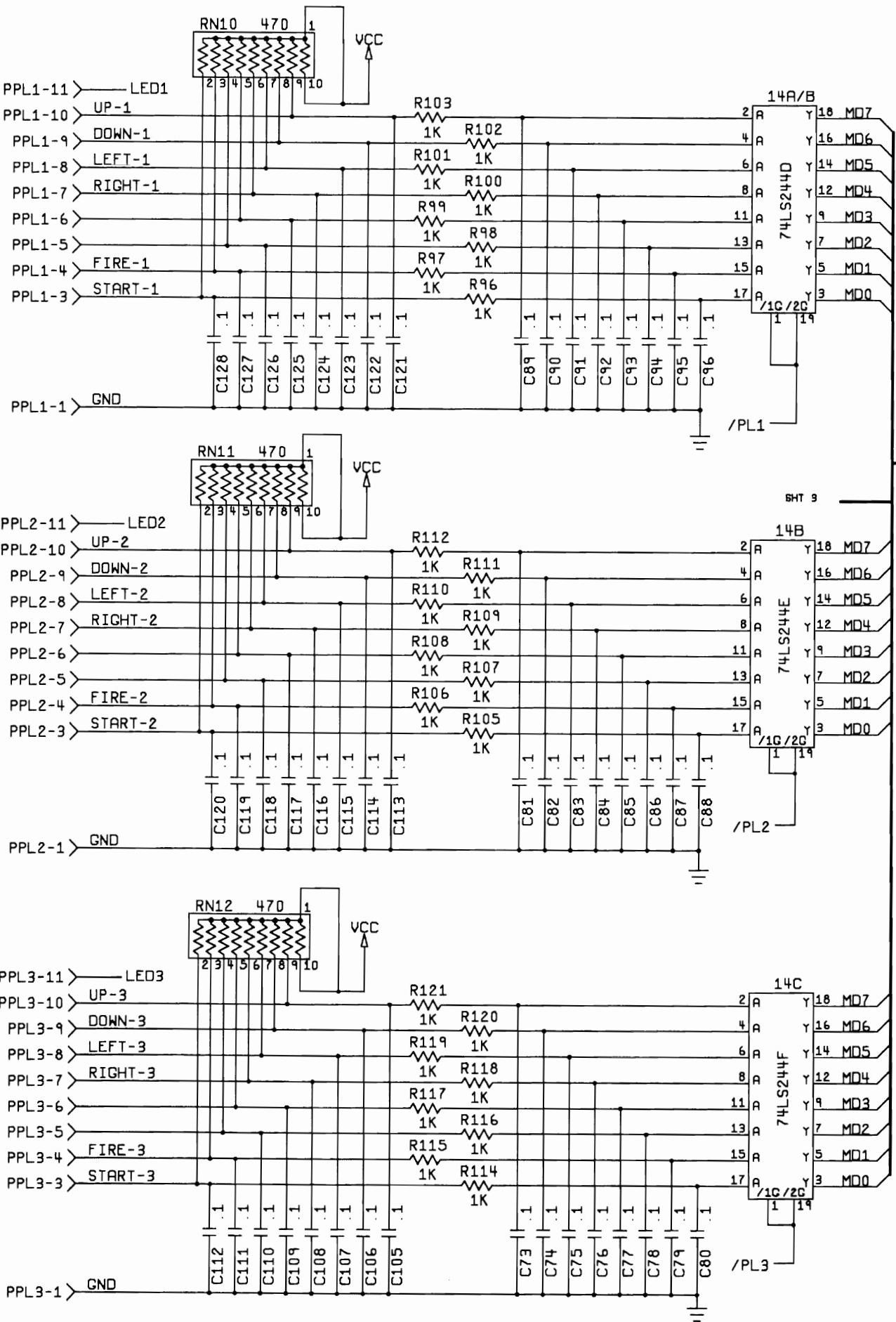


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**Gauntlet™ Game PCB
Schematic Diagram**



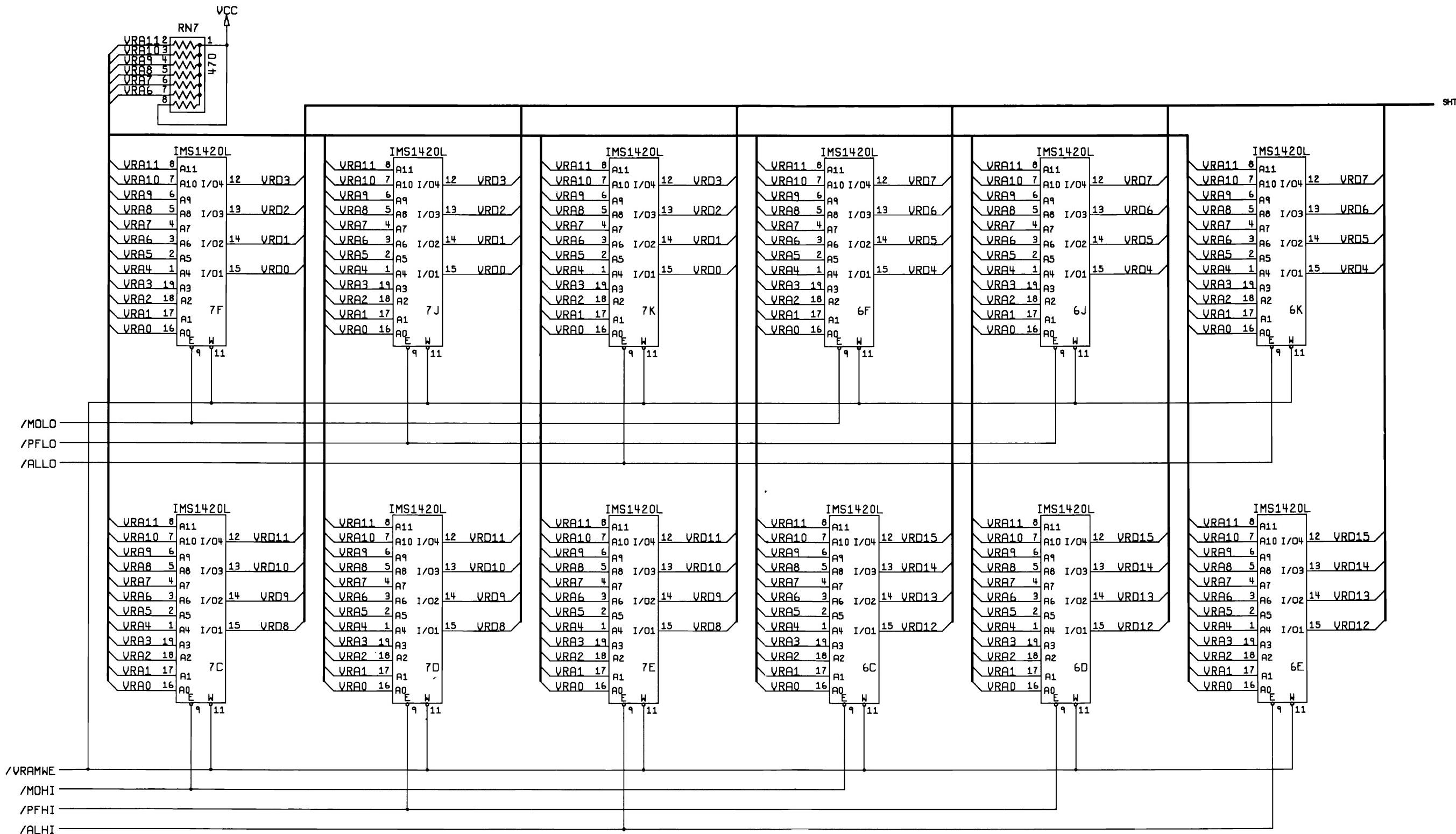
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Gauntlet™ Game PCB Schematic Diagram





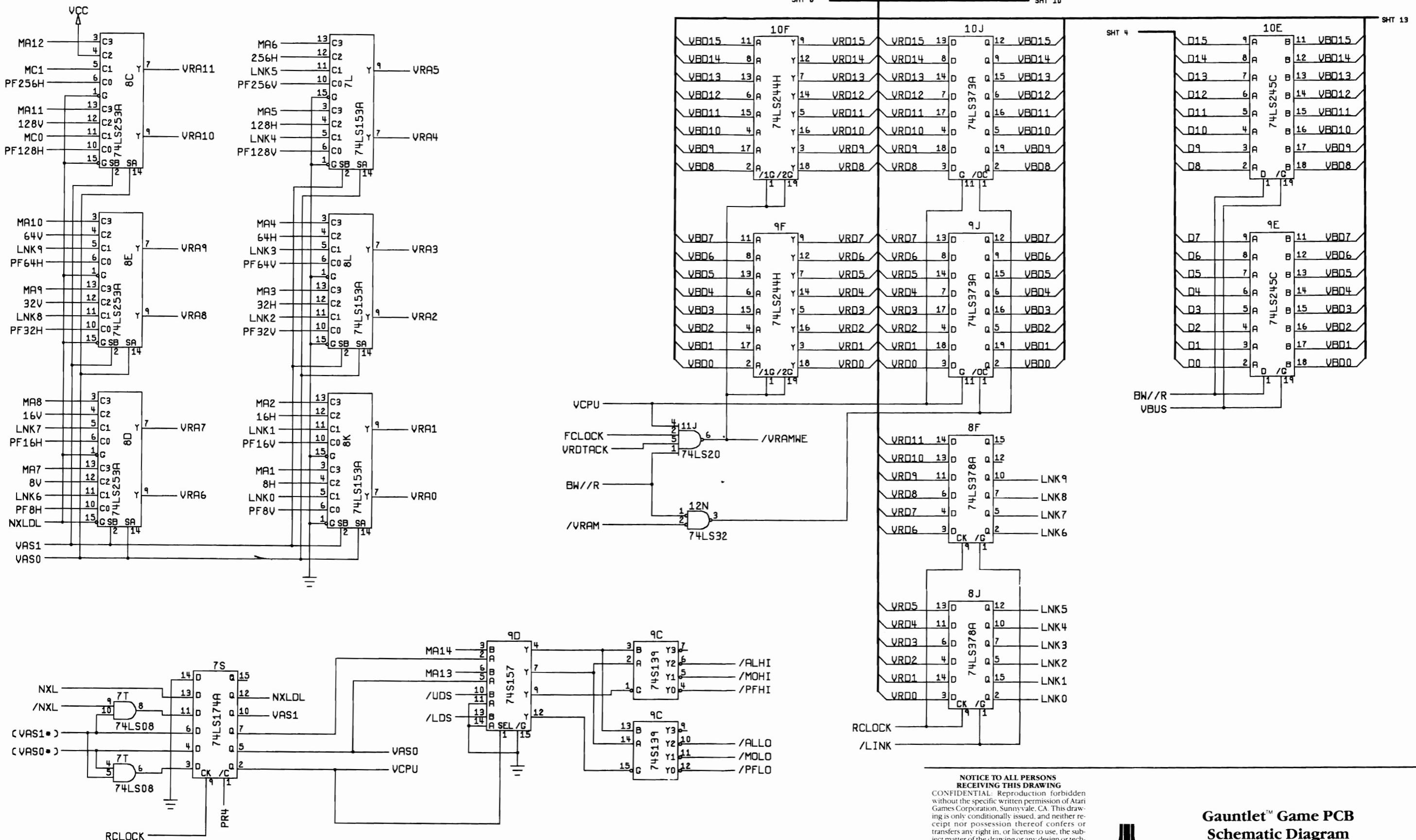
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Gauntlet™ Game PCB
Schematic Diagram

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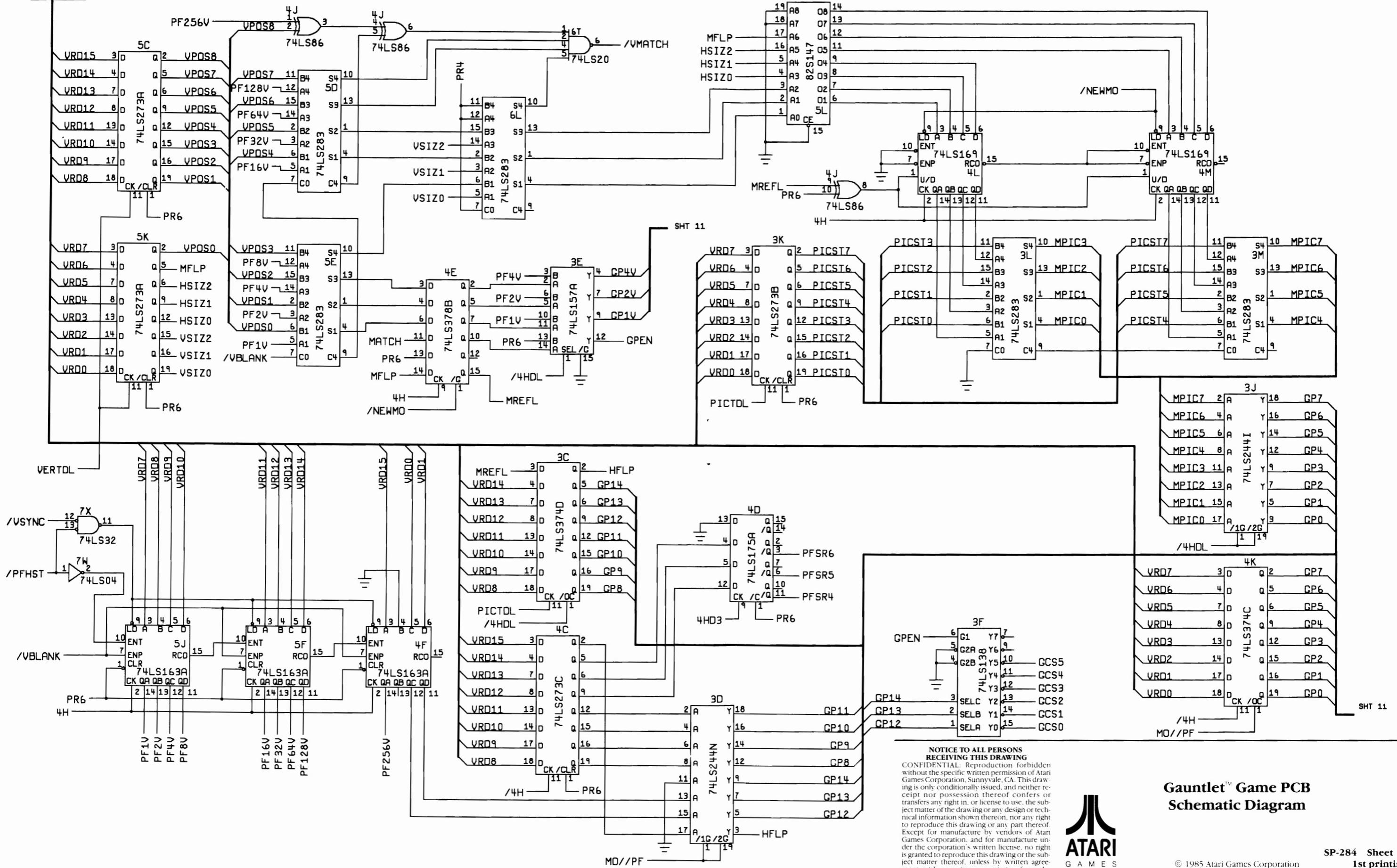


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Gauntlet™ Game PCB Schematic Diagram



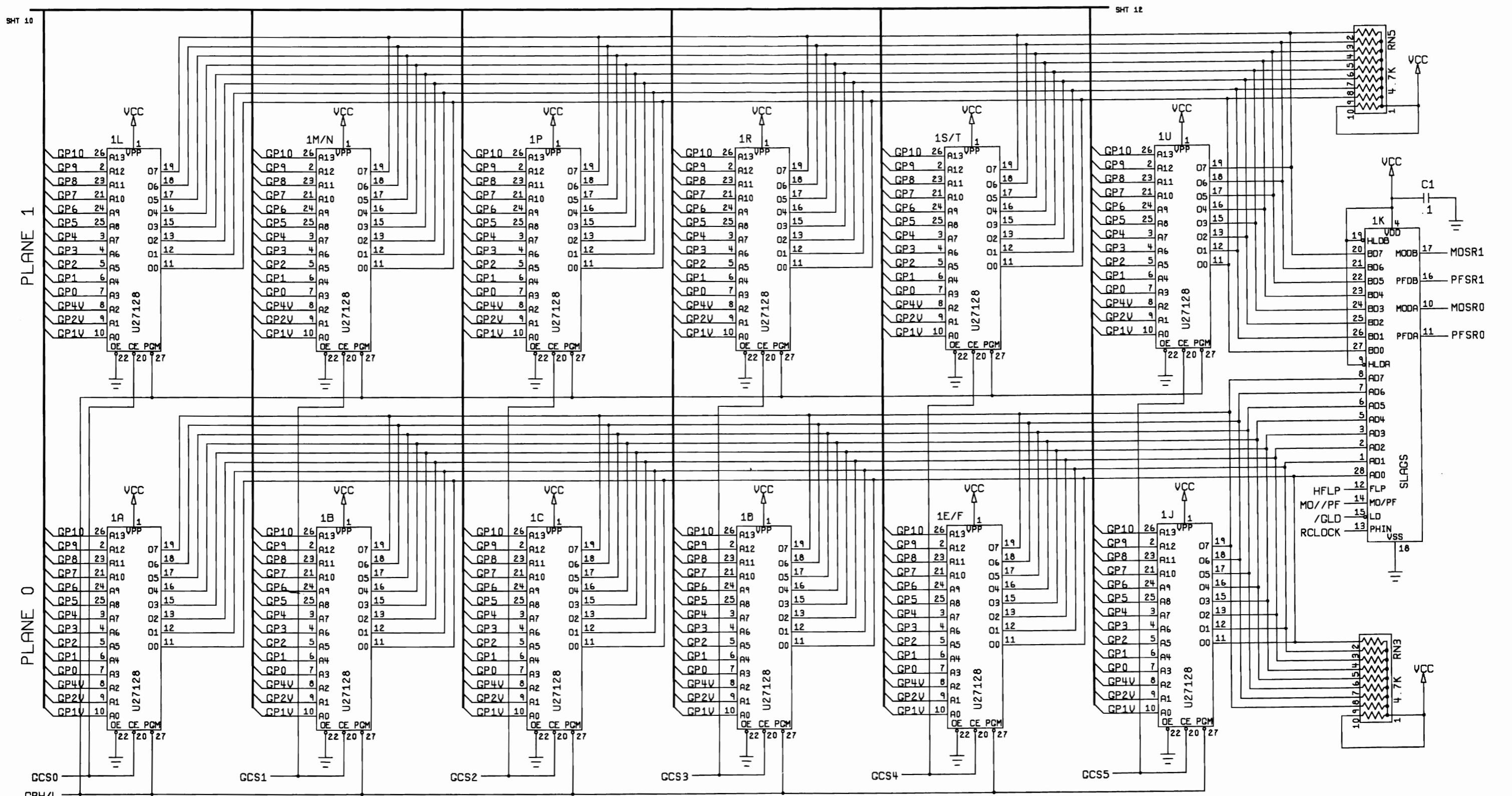
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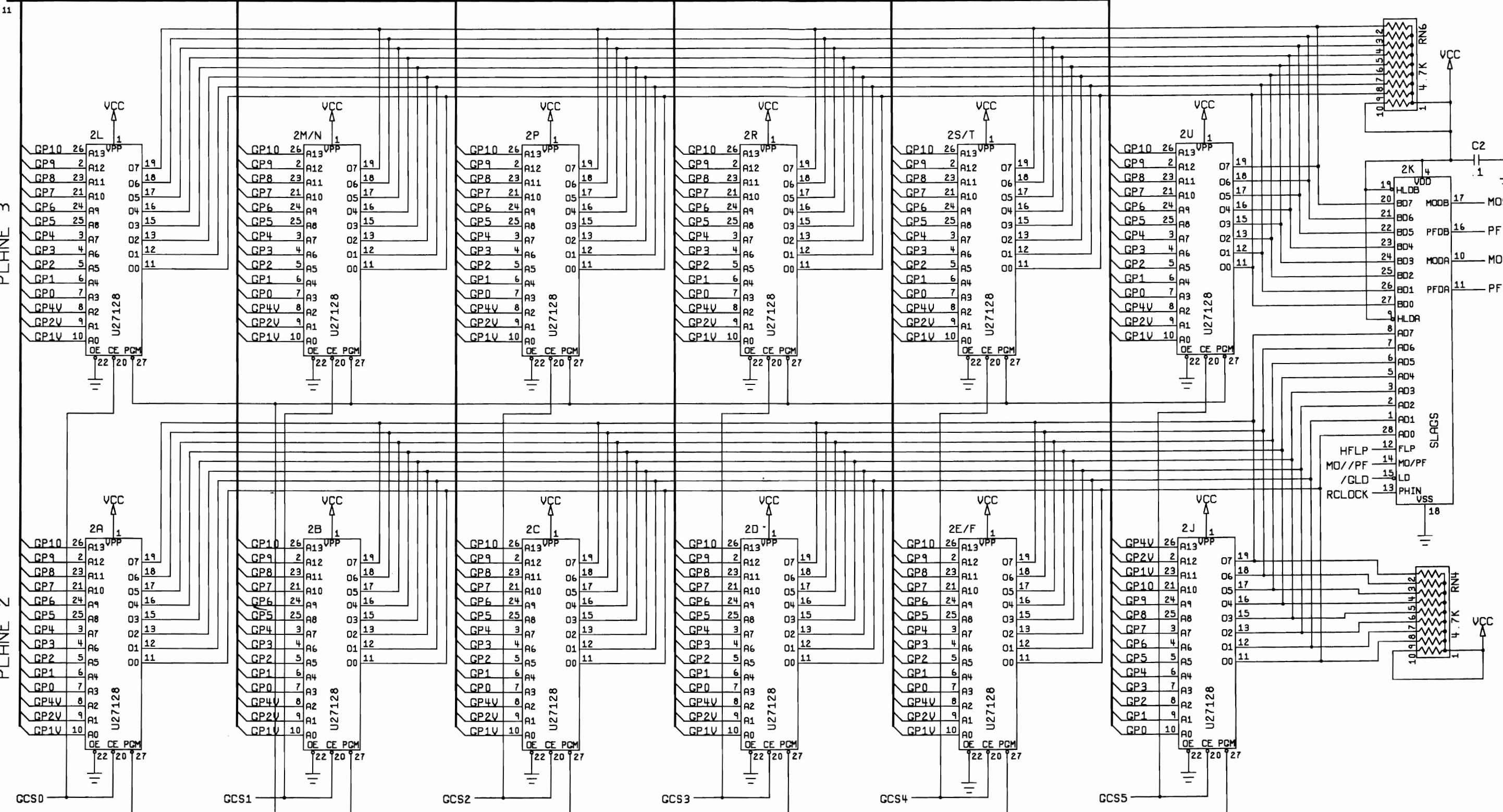


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Schematic Diagram**

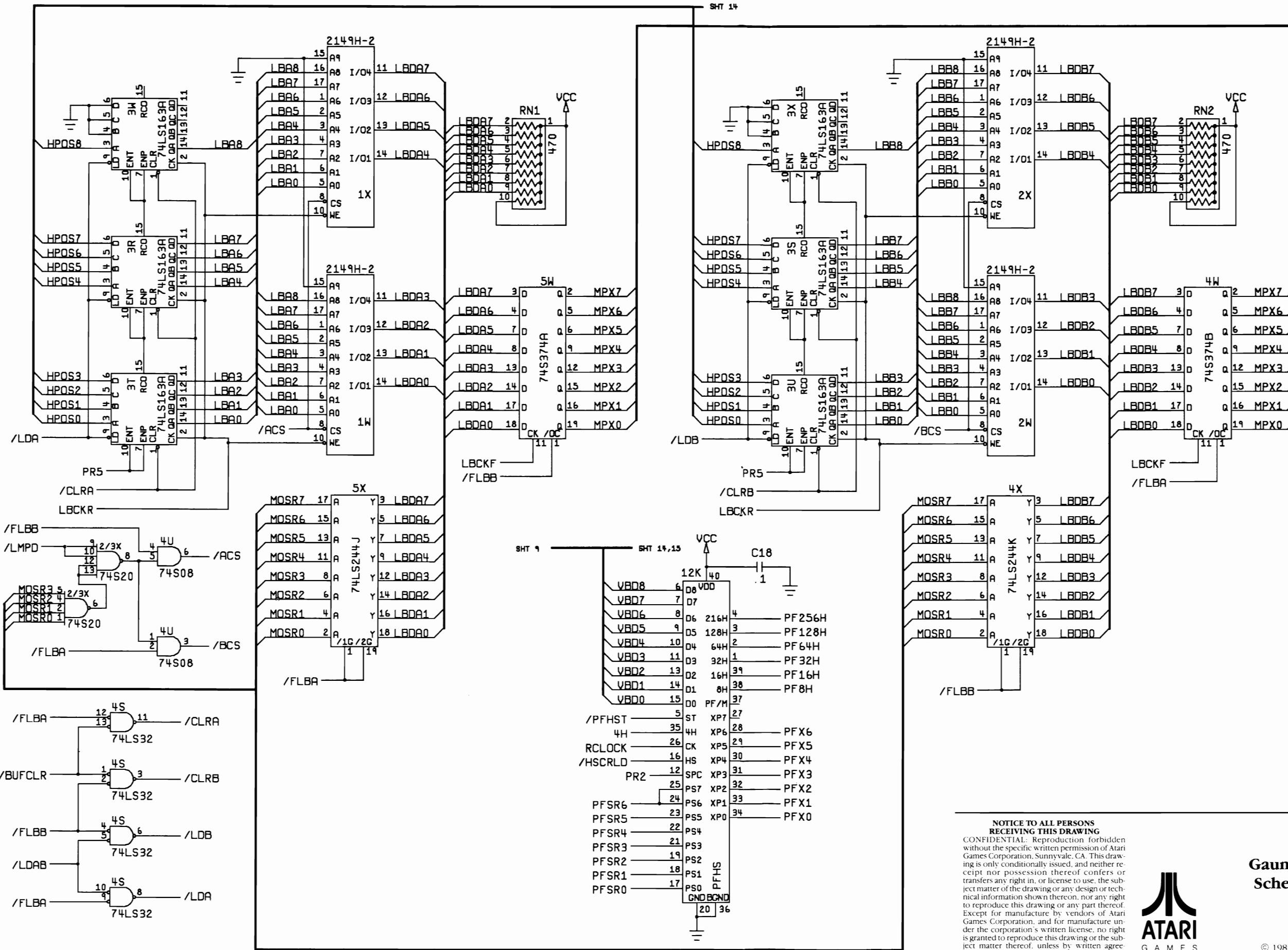


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Gauntlet™ Game PCB Schematic Diagram



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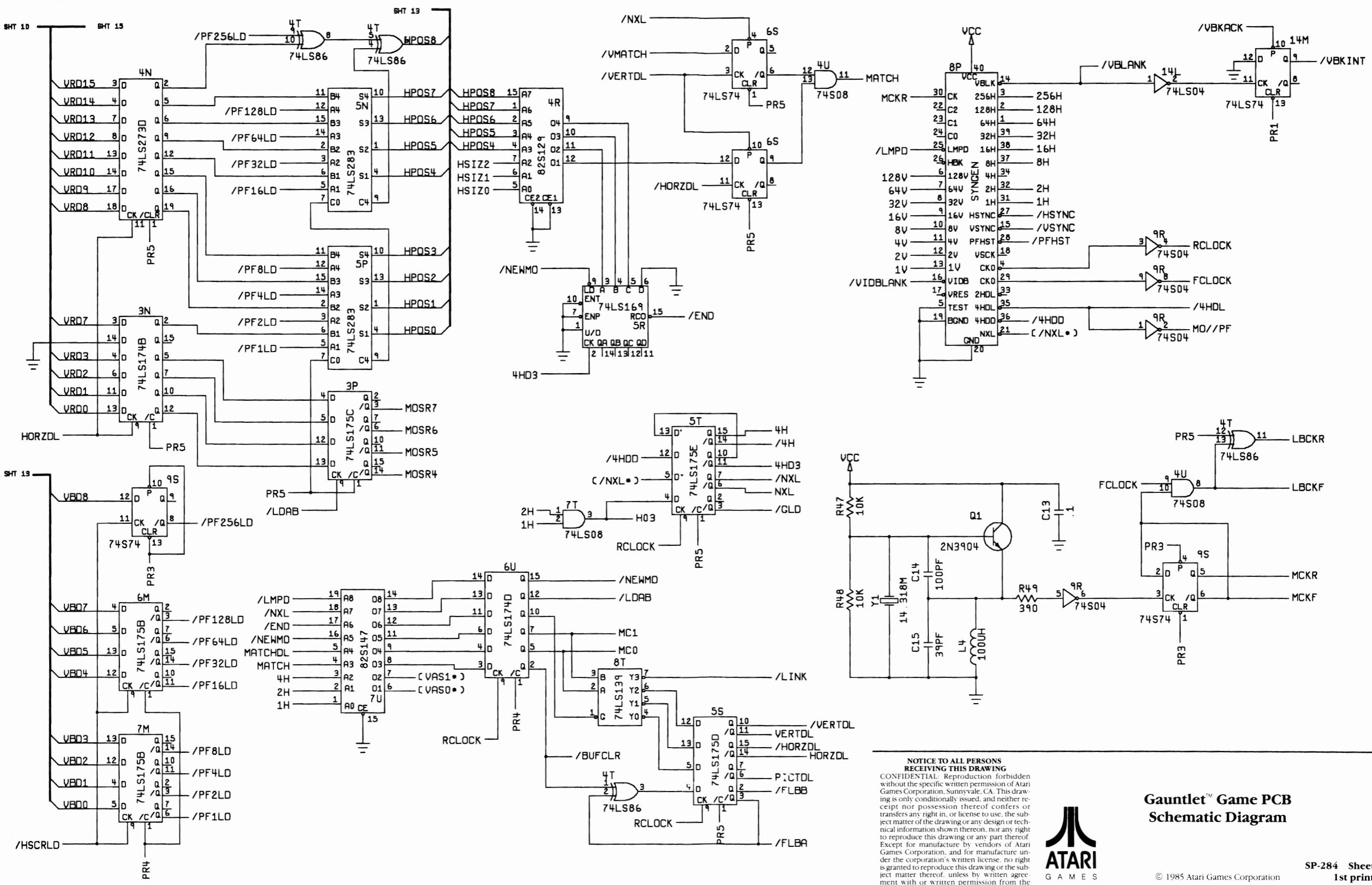


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Gauntlet™ Game PCB Schematic Diagram



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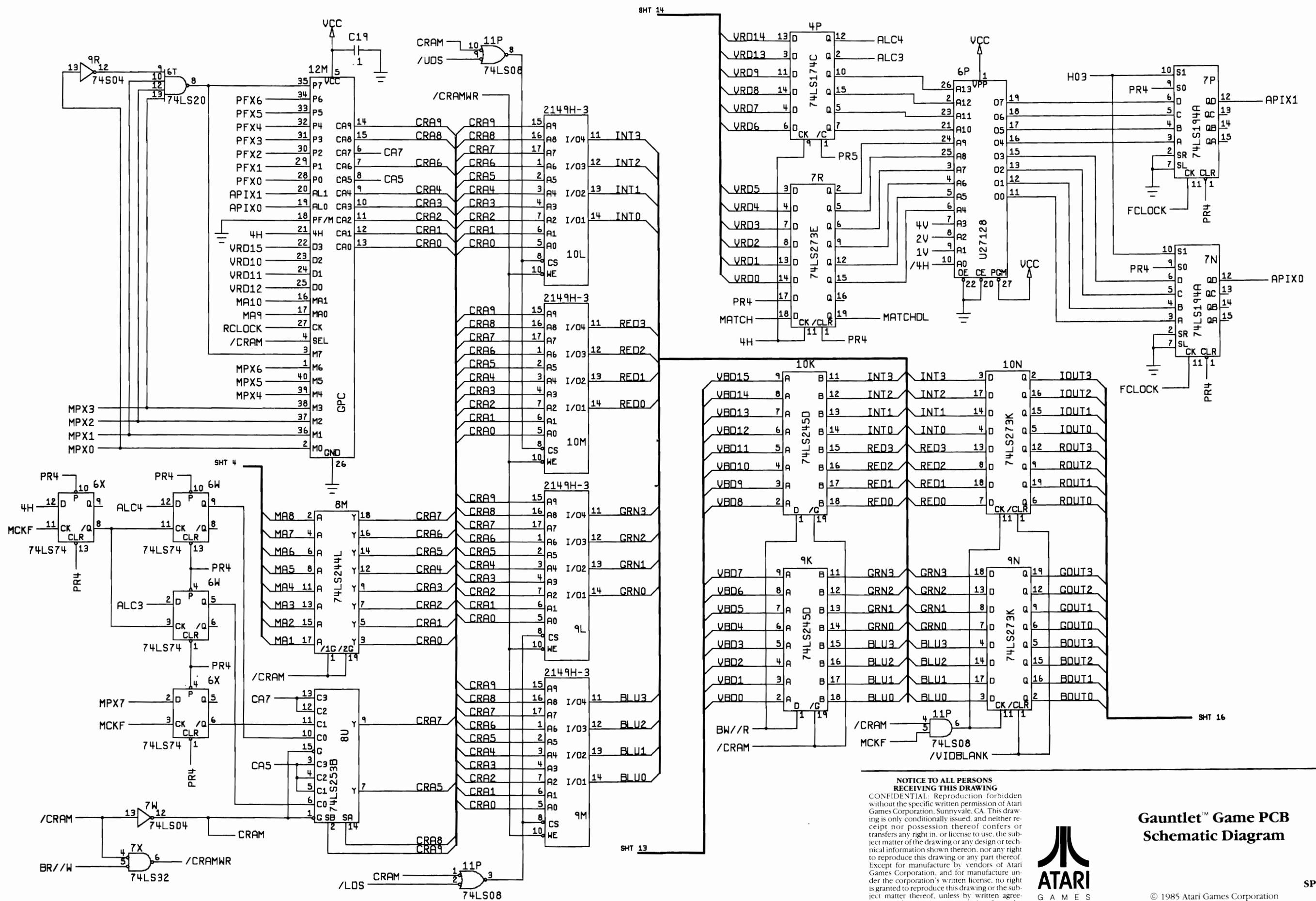


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**Gauntlet™ Game PCB
Schematic Diagram**



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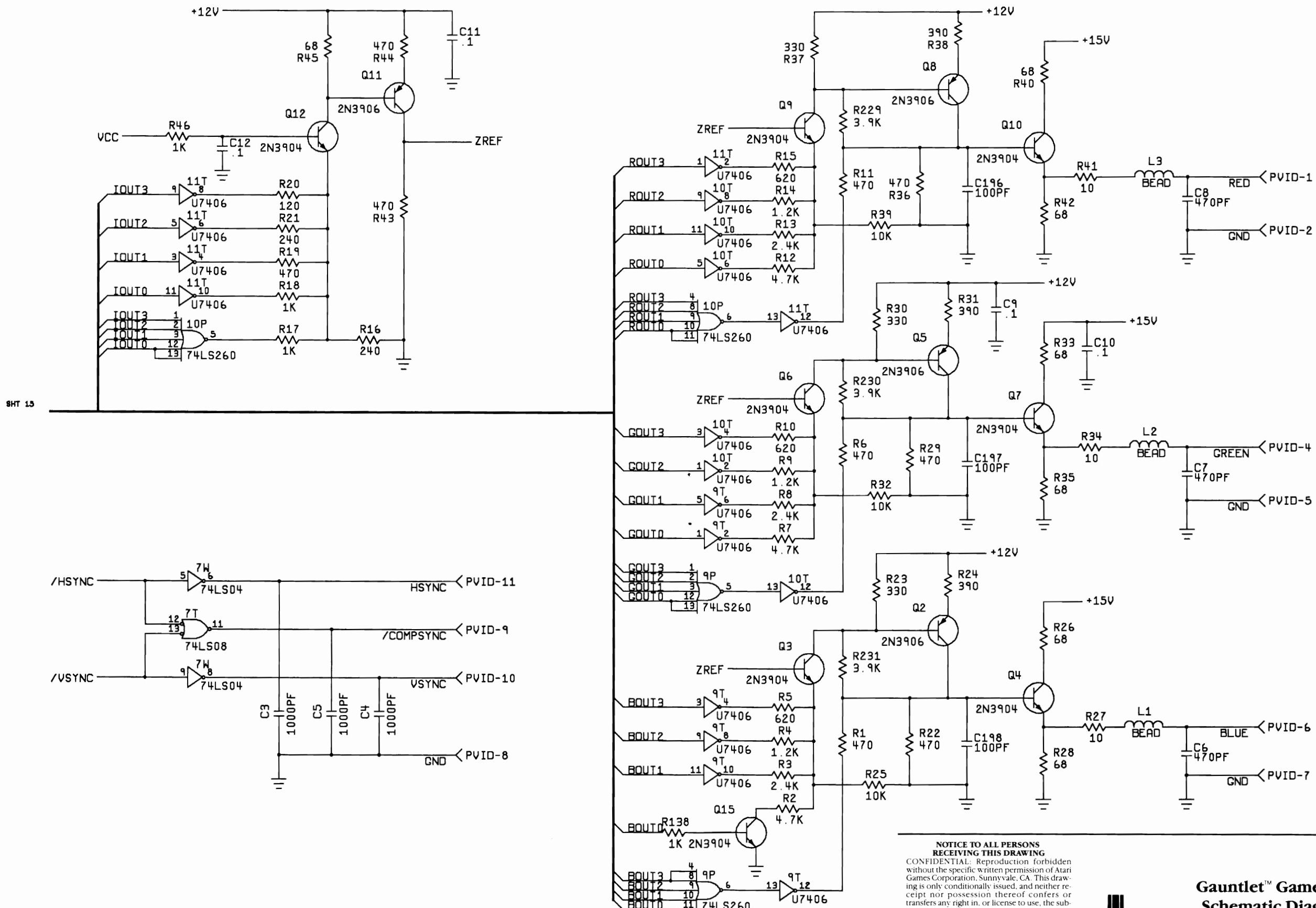


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Gauntlet™ Game PCB
Schematic Diagram



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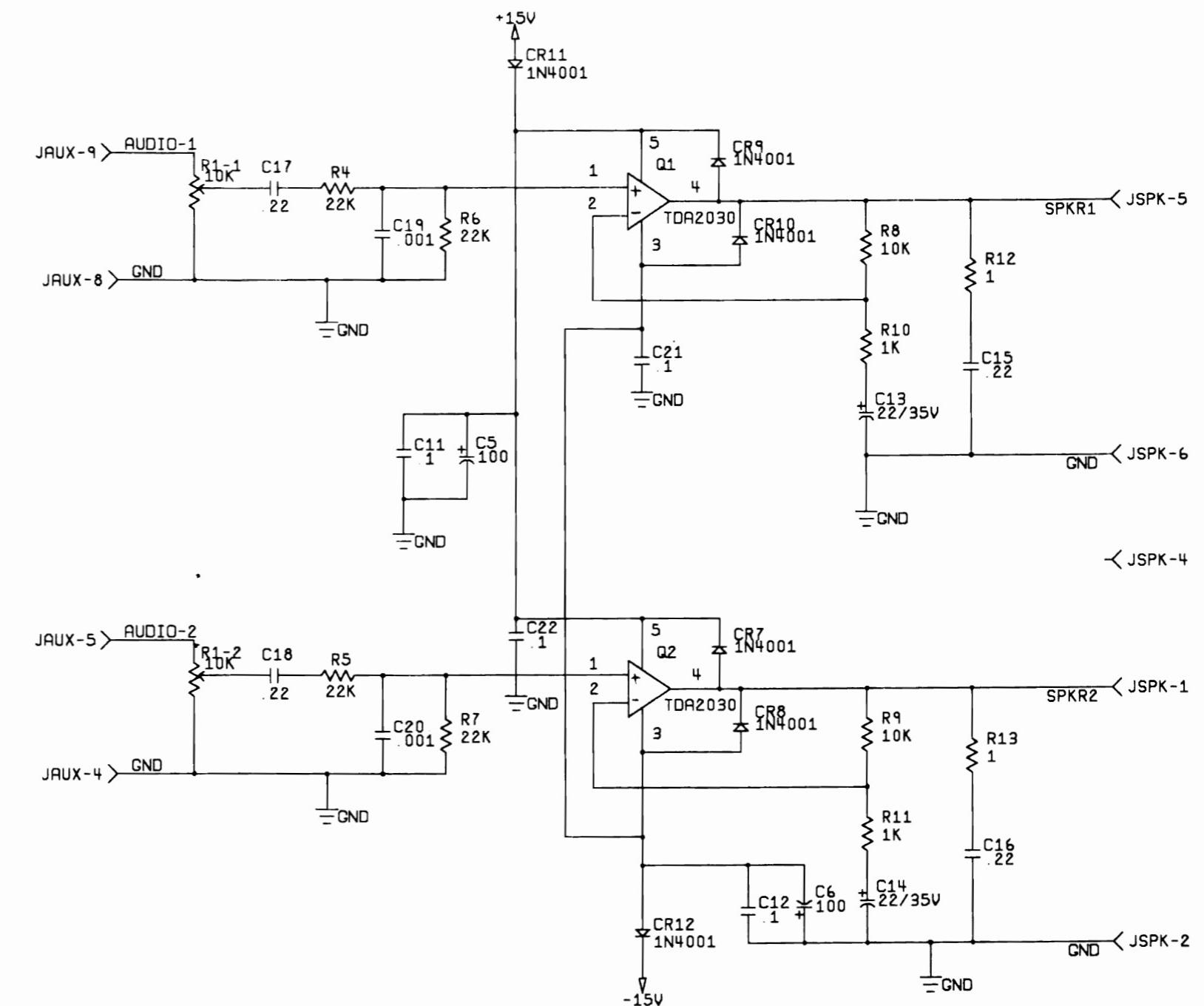
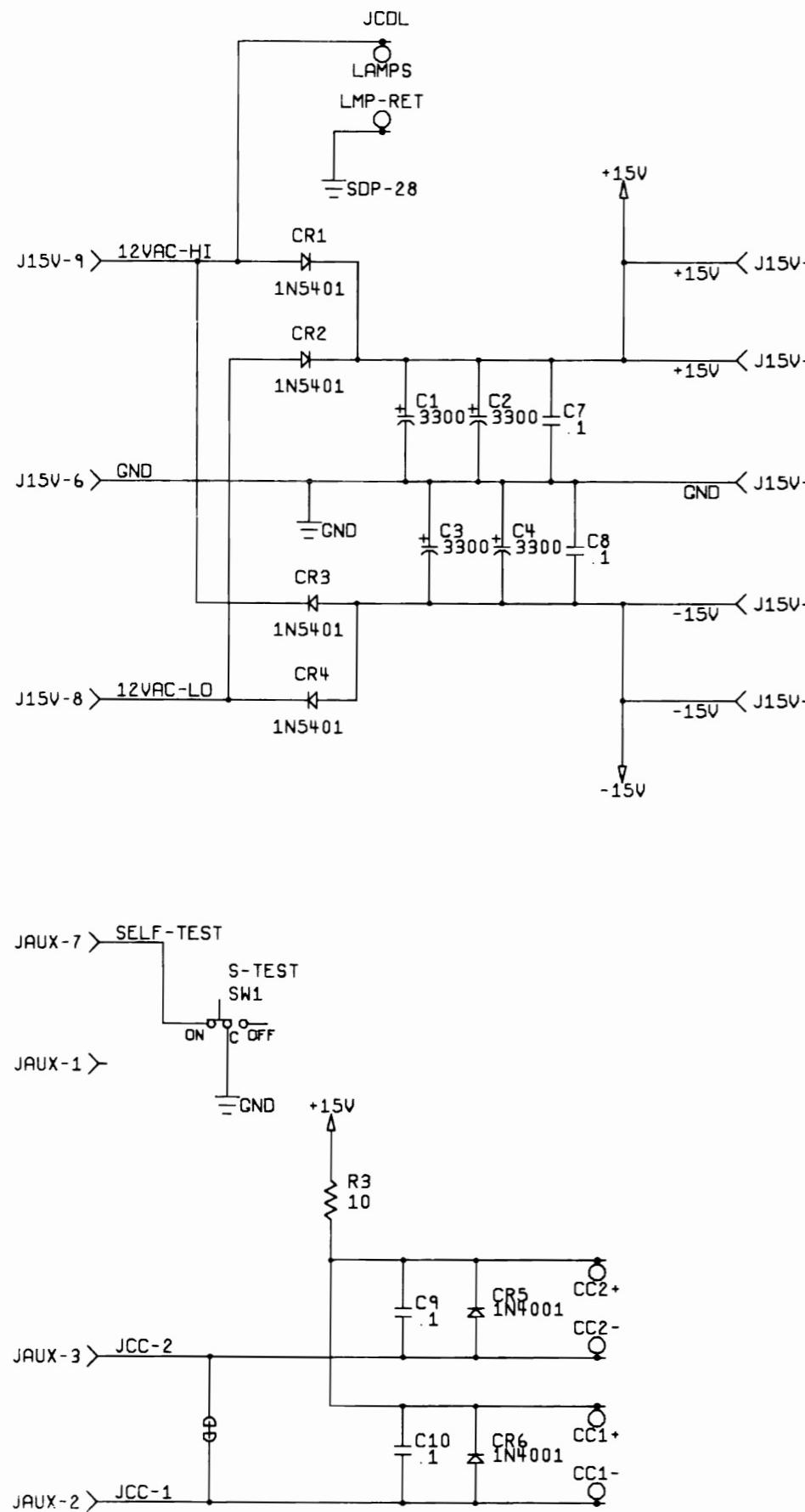


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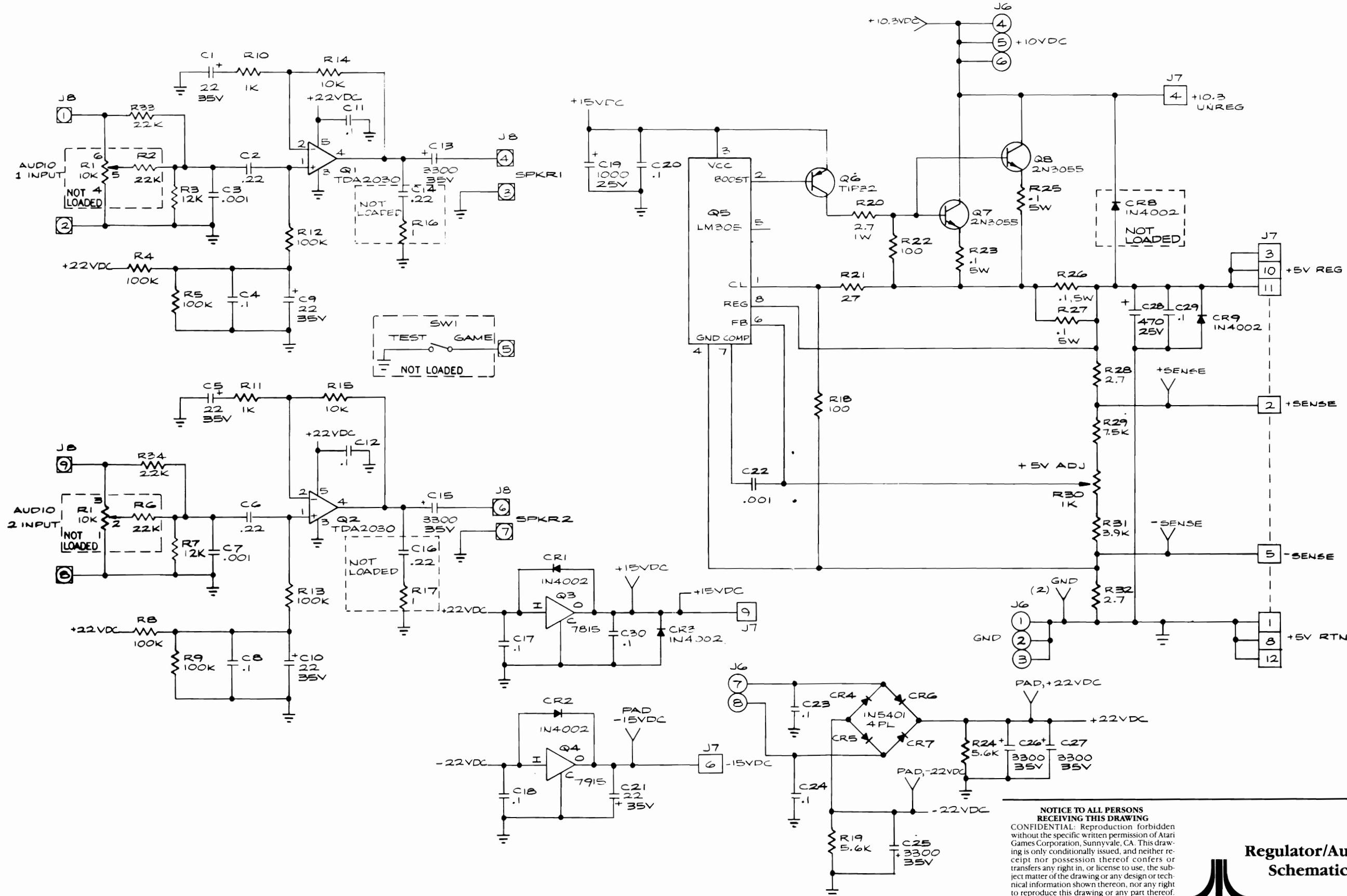


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Audio PCB Assembly Schematic Diagram (U.S.)



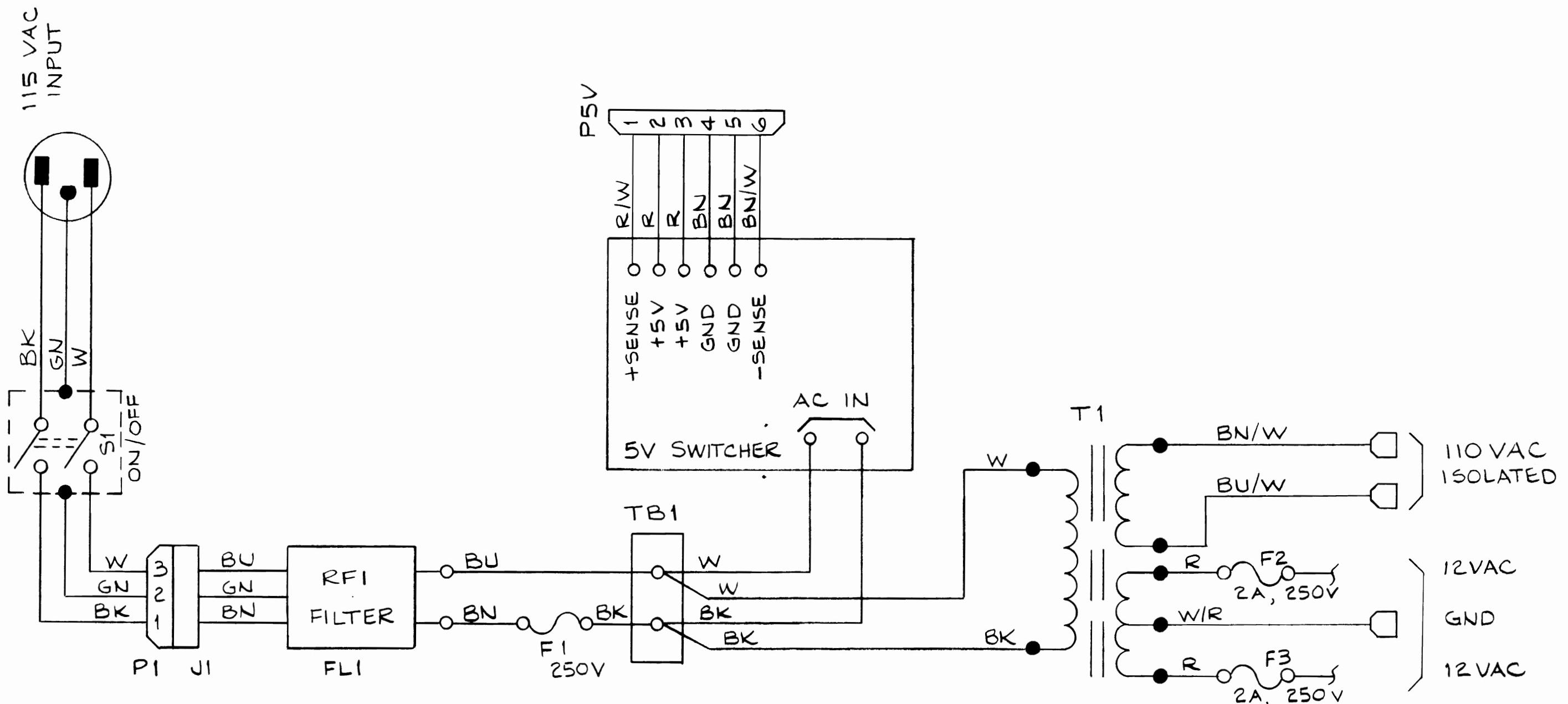
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**Regulator/Audio III PCB Assembly
Schematic Diagram (Ireland)**

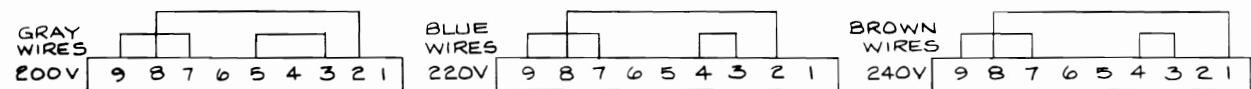


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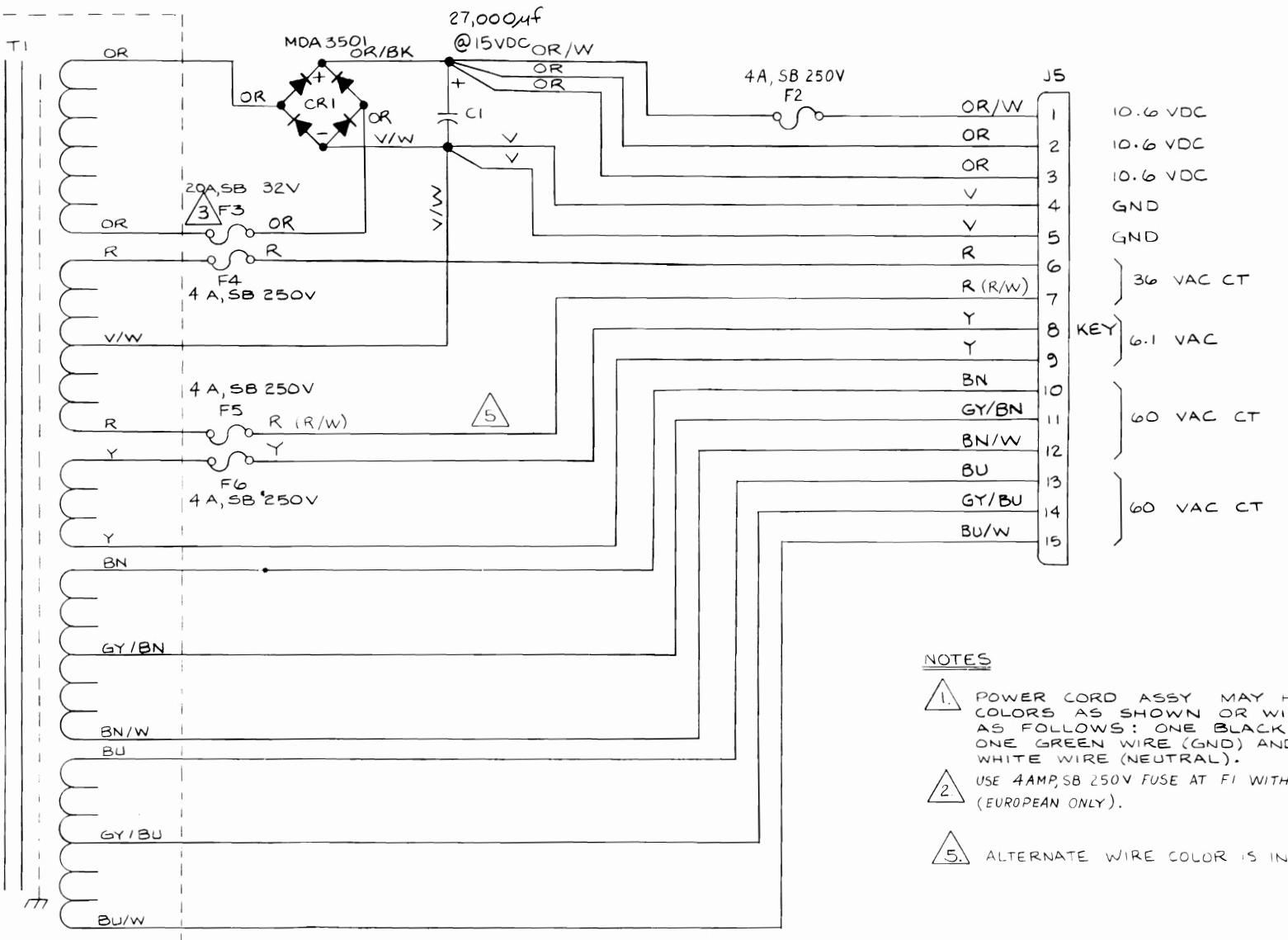
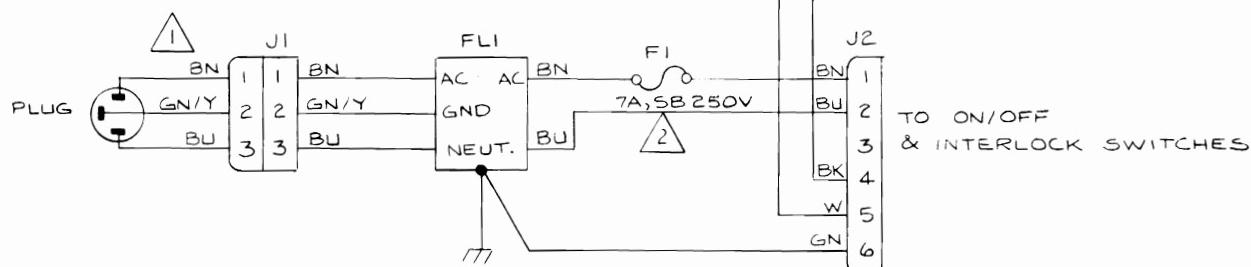
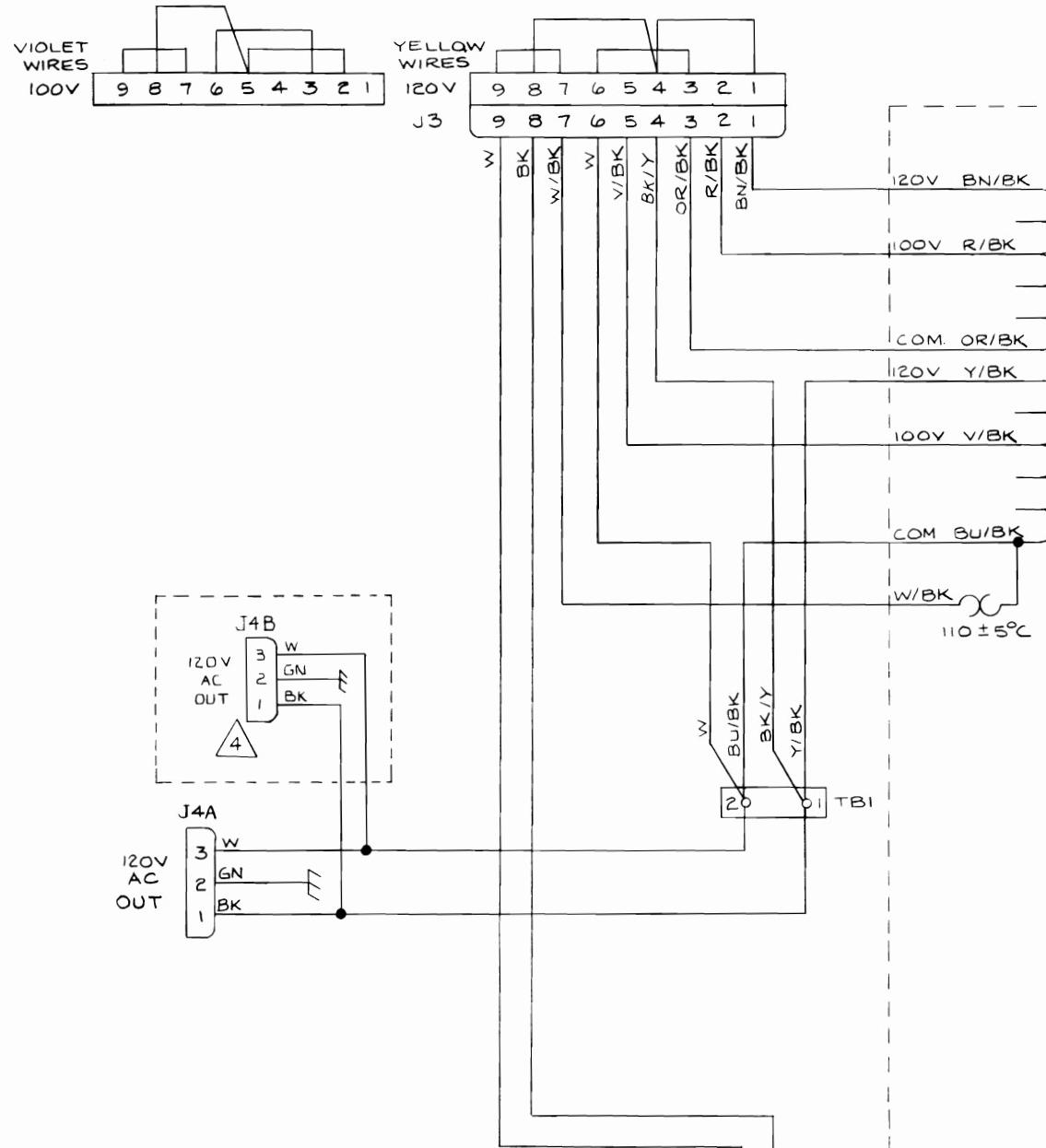
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Switching/Linear (SL) Power Supply Wiring Diagram (U.S.)





VOLTAGE SELECTION BLOCKS



NOTES

**! POWER CORD ASSY MAY HAVE WIRE
COLORS AS SHOWN OR WIRE COLORS
AS FOLLOWS: ONE BLACK WIRE (AC),
ONE GREEN WIRE (GND) AND ONE
WHITE WIRE (NEUTRAL).**

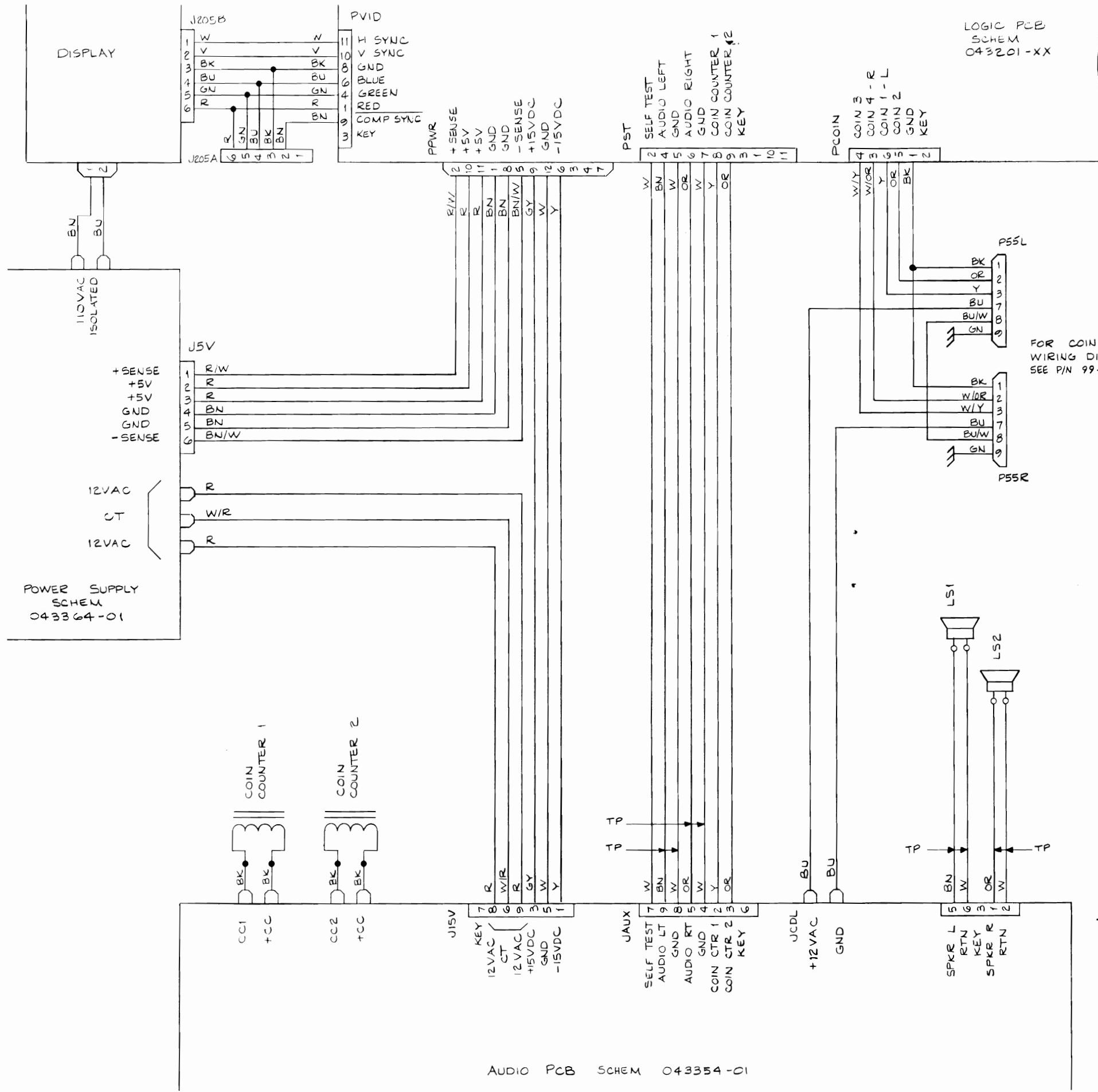
2 USE 4AMP,SB 250V FUSE AT F1 WITH 220V & 240V
(EUROPEAN ONLY).

5. ALTERNATE WIRE COLOR IS IN PARENTHESES ().

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Linear Power Supply Wiring Diagram (Ireland)

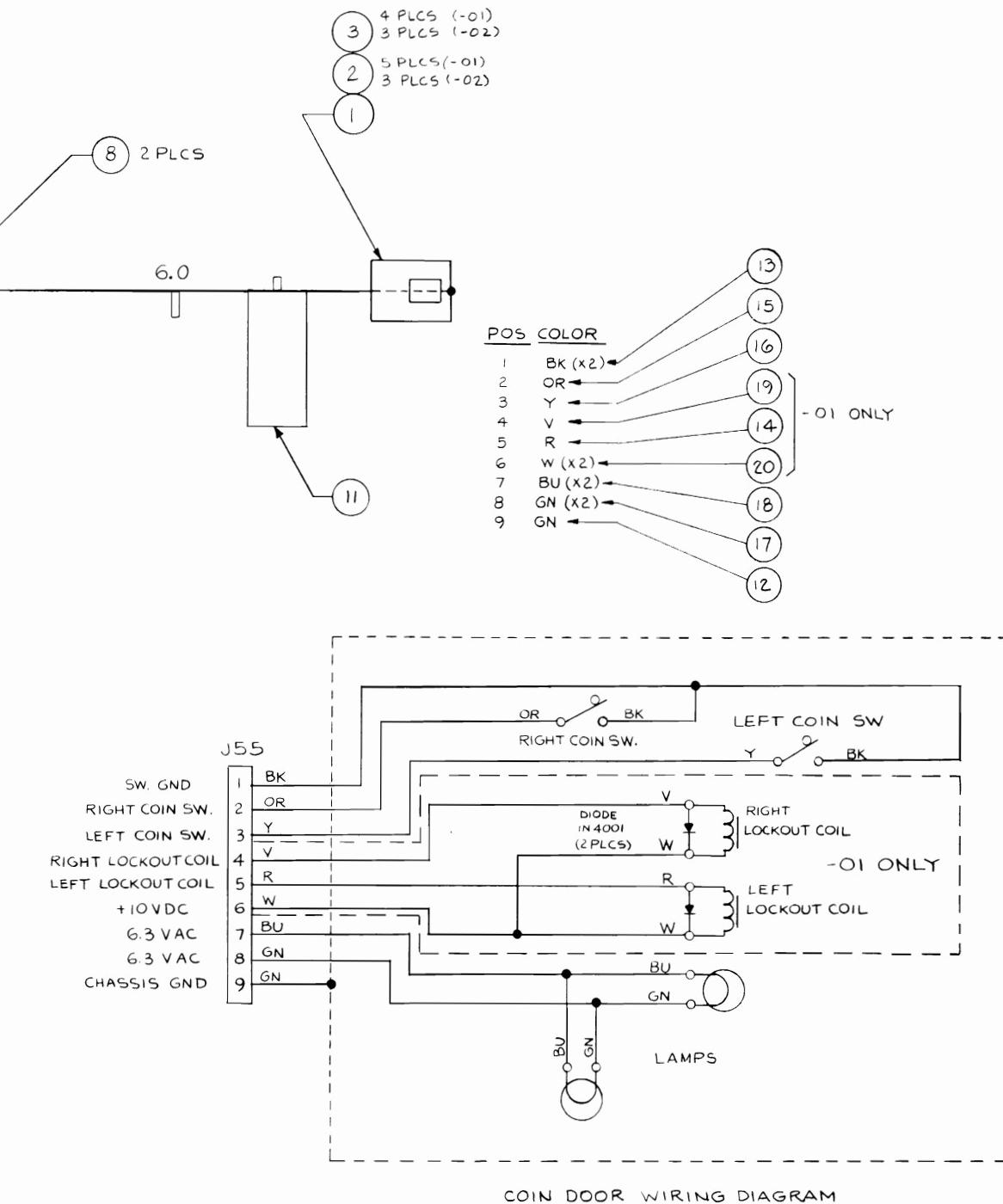
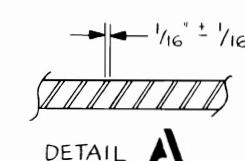
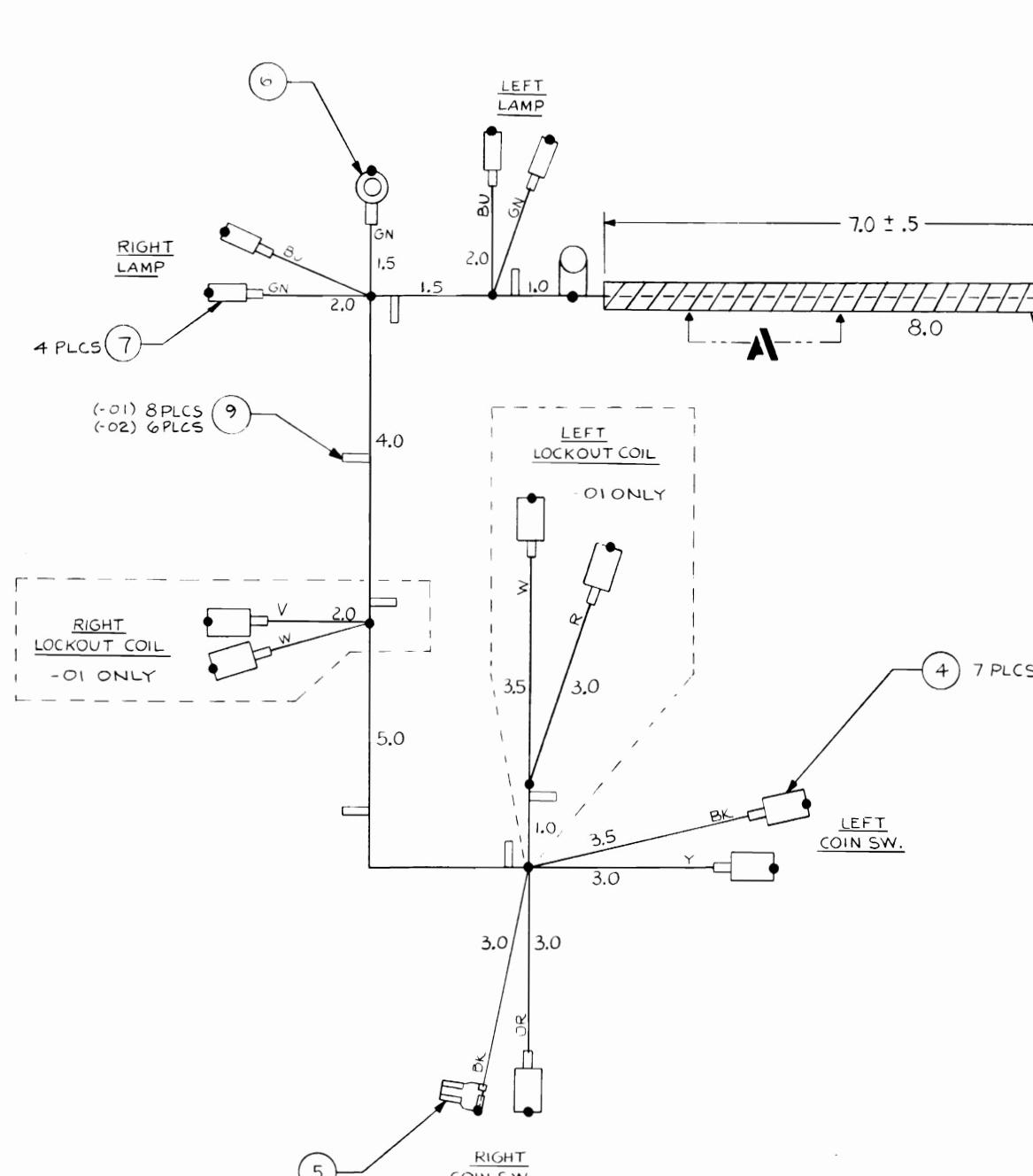


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Gauntlet™ Game Wiring Diagram





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Coin Door Wiring Diagram



Gauntlet™ 68010 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program ROM/Operating System	000000-00FFFF	R	D0-D15
Program ROM/SLAPSTIC	038000-03FFFF	R	D0-D15
Program ROM/Main	040000-07FFFF	R	D0-D15
Spare RAM	800000-801FFF	R/W	D0-D15
EEPROM	802001-802FFF	R/W	D7-D0
Player 1 Input (see detail below)	803001	R	D0-D71
Player 2 Input	803003	R	D0-D7
Player 3 Input	803005	R	D0-D7
Player 4 Input	803007	R	D0-D7
<i>Player Inputs:</i>			
Joystick Up			D7
Joystick Down			D6
Joystick Left			D5
Joystick Right			D4
Spare			D3
Spare			D2
Fire			D1
Magic/Start			D0
VBLANK (Active Low)	803009	R	D6
Output/Buffer Full (@ 803170) (Active High)	803009	R	D5
Input/Buffer Full (@ 80300F) (Active High)	803009	R	D4
Self-Test (Active Low)	803009	R	D3
Read Sound Processor (6502)	80300F	R	D0-D7
Watchdog (128 msec. timeout)	803100	W	xx
LED-1 (Low On)	803121	W	D0
LED-2 (Low On)	803123	W	D0
LED-3 (Low On)	803125	W	D0
LED-4 (Low On)	803127	W	D0
Sound Processor Reset (Low Reset)	80312F	W	D0
VBlank Acknowledge	803140	W	xx
Unlock EEPROM	803150	W	xx
Write Sound Processor (6502)	803171	W	D0-D7
Playfield RAM	900000-901FFF	R/W	D0-D15
Motion Object Picture	902000-9027FF	R/W	D0-D15
Motion Object Horizontal Position	902800-902FFF	R/W	D0-D15
Motion Object Vertical Position	903000-9037FF	R/W	D0-D15
Motion Object Link	903800-903FFF	R/W	D0-D15
Spare RAM	904000-904FFF	R/W	D0-D15
Alphanumerics RAM	905000-905FFF	R/W	D0-D15
Playfield Vertical Scroll	905F6E, 905F6F	R/W	D7-D15
Playfield ROM Bank Select	905F6F	R/W	D0, D1
Color RAM Alpha	910000-9101FF	R/W	D0-D15
Color RAM Motion Object	910200-9103FF	R/W	D0-D15
Color RAM Playfield Shadow	910400-9104FF	R/W	D0-D15
Color RAM Playfield	910500-9105FF	R/W	D0-D15
Color RAM (Spare)	910600-9107FF	R/W	D0-D15
Playfield Horizontal Scroll	930000, 930001	W	D0-D8

NOTE

All addresses can be accessed in byte or word mode.

Gauntlet™ 6502 Memory Map

FUNCTION	ADDRESS	R/W	DATA
Program RAM	0000-0FFF	R/W	D0-D7
Write 68010 Port (Output Buffer)	1000	W	D0-D7
Read 68010 Port (Input Buffer)	1010	R	D0-D7
<i>Audio Mix:</i>			
Speech Mix	1020	W	D5-D7
Effects Mix	1020	W	D3, D4
Music Mix	1020	W	D0-D2
Coin 1 (Left)	1020	R	D3
Coin 2	1020	R	D2
Coin 3	1020	R	D1
Coin 4 (Right)	1020	R	D0
Data Available (@ 1010) (Active High)	1030	R	D7
Output Buffer Full (@ 1000) (Active High)	1030	R	D6
Speech Ready (Active Low)	1030	R	D5
Self-Test (Active Low)	1030	R	D4
Music Reset (Low Reset)	1030	W	D7
Speech Write (Active Low)	1031	W	D7
Speech Reset (Active Low)	1032	W	D7
Speech Squeak (Low = 650KHz Clock)	1033	W	D7
Coin Counter Right (Active High)	1034	W	D7
Coin Counter Left (Active High)	1035	W	D7
Effects	1800-180F	R/W	D0-D7
Music	1810-1811	R/W	D0-D7
Speech	1820	W	D0-D7
Interrupt Acknowledge	1830	R/W	xx
Program ROM (48k bytes)	4000-FFFF	R	D0-D7

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Gauntlet™ 68010 and 6502 Microprocessor Memory Maps

Gauntlet Signal Name Glossary

2.5V	2.5 volts audio amplifier reference
+5AUD	5 volts audio amplifier reference
10.3V	Power-on-reset control voltage
+12V	+ 12 volts regulated
+15V	+ 15 volts unregulated
-15V	- 15 volts unregulated
-5V	- 5 volts regulated
1H-256H	Screen horizontal address counter chain
1V-128V	Screen vertical address counter chain
4H	Inverted 4H signal
4HD3, 4HD3	4H signal delayed three clock cycles
4HDD	4H signal delayed two clock cycles
4HDL	4H signal delayed one clock cycle
68KBUF	68010 output buffer full (to 6502)
A1-A23	68010 address bus unbuffered
ACS	"A" line buffer RAMs chip select
ALC3, ALC4	Alphanumeric palette data bits 3 and 4
ALHI, ALLO	Alphanumeric RAM chip selects
APIX0, APIX1	Alphanumeric pixel data
AS	68010 address strobe
AUDIO-L, AUDIO-R	Left and right audio outputs (5V peak-to-peak)
B02	6502 buffered phase 2 (Φ_2)
BAS	Buffered address strobe (see AS)
BCS	"B" line buffer RAMs chip select
BLU0-BLU3	Blue color RAM data
BLUE	Blue analog video output
BOUT0-BOUT3	Blue latched digital video output
BR/W	68010 read/write control, buffered
BUFCLR	Swap "A" and "B" line buffers, clear line buffer counter chain
BW/R	68010 read/write inverted, buffered
CA5, CA7	Color RAM address bits 5 and 7
CCTR1, CCTR2	Coin counter outputs 1 and 2.
CLRA	Clear line buffer "A" address counters
CLRB	Clear line buffer "B" address counters

NOTE

In this signal name glossary all active-low signals are over-scored, e.g., COMPSYNC. In the schematics printed on Sheets 1-16 a slash (/) in front of a signal name indicates an active-low signal.

Gauntlet Signal Name Glossary, continued

COIN	Coin input buffer chip select	HSIZ0-HSIZ2	Motion object horizontal size	MIX	Latch audio mix data
COIN1-L, COIN2, COIN3, COIN4-R	Four coin switch inputs	H SYNC, H SYNC	Horizontal sync output	MO/PF	Motion object or playfield picture select
COMPSYNC	Negative composite sync output	INPUT	68010 miscellaneous inputs buffer select	MOHI, MOLO	Motion object RAM chip selects
CRA0-CRA9	Color RAM address	INT0-INT3	Color intensity RAM data	MOSR0-MOSR3	Motion object pixel data, before the line buffers
CRAM, CRAM	68010 address decode for color RAM	IOUT0-IOUT3	Intensity latched digital video output	MOSR4-MOSR7	Motion object pixel palette data, before the line buffers
CRAMWR	Color RAM write enable	LATCH	68010 miscellaneous latched outputs chip select		The lower 8 bits of the motion object picture address
D0-D15	68010 data bus, unbuffered	LAUD	Summed left channel audio	MPIC0-MPIC7	Motion object stamp horizontal flip state
DOWN-1-DOWN-4	Joystick down switch inputs, players 1-4	LBA0-LBA8	Line buffer "A" address bus	MPX0-MPX7	Music chip select
EEPROM	Electrically erasable PROM chip select	LBB0-LBB8	Line buffer "B" address bus		Start a new motion object
END	Current motion object finished	LBCKF	Line buffer clock inverted phase	MREFL	Next line
FCLOCK	System clock inverted phase	LBCKR	Line buffer clock	MUSIC	NXL one clock cycle early
FIRE-1-FIRE-4	Fire switch inputs, players 1-4	LBDA0-LBDA7	Line buffer "A" data bus	NEWMO	NXL delayed one clock cycle
FLBA	Line buffer "A" fill control	LBDB0-LBDB7	Line buffer "B" data bus	NXL, NXL	Latched playfield horizontal scroll data
FLBB	Line buffer "B" fill control	LDA	Load line buffer "A" address counters	(NXL*)	Playfield vertical address counter chain
GCS0-GCS5	Graphics ROMs chip select	LDAB	Load line buffer "A" or "B" address counters	NXL_DL	Playfield horizontal address counter chain
GLD	Graphics load (to SLAGS chips)	LDB	Load line buffer "B" address counters	PF1LD-PF256LD	Playfield picture bank select
GND	System ground	LDS	68010 lower data strobe	PF1V-PF256V	Playfield RAM chip selects
GOUT0-GOUT3	Green latched digital video output	LED1-LED4	LED outputs, players 1-4	PF8H-PF256H	Playfield scroll control
GP0-GP14	Graphics picture address	LEFT-1-LEFT-4	Joystick left switch inputs, players 1-4	PFBANK0, PFBANK1	Playfield pixel data, before PFHS
GP1V, GP2V, GP4V	Graphics picture stamp sub-address	LINK	Latch motion object link data	PFHI, PFLO	Playfield pixel palette data, before PFHS
GOPEN	Graphics picture enable	LMPD	Stop motion object processing for line buffer changeover	PFHST	Playfield pixel data after PFHS
GREEN	Green analog video output	LNK0-LNK9	Motion object link data	PFSR0-PFSR3	Motion object start address
GRH/L	Graphics ROM high/low select (A14 on a 27256)	MA1-MA14	68010 address bus buffered	PFSR4-PFSR6	Latch motion object picture data
GRN0-GRN3	Green color RAM data	MATCH	Motion object H and V data matches current playfield position	PFX0-PFX6	PICT delayed one clock cycle
H03	Alphanumeric load (to shift registers)	MATCHDL	Previous MATCH state	PICST0-PICST7	Effects chip audio
HFLP	Graphics stamp horizontal flip	MBUS	68010 "M" data bus buffers enable	PICTDL	Player input chip selects, players 1-4
HORZ	Latch motion object horizontal data and palette data	MC0, MC1	Motion object parameter control select	PKAUD	Effects audio mix control bits
HORZDL, HORZDL	HORZ delayed one clock cycle	MCEN	Motion object parameter control enable	PL1-PL4	Effects chip select
HPOS0-HPOS8	Motion object horizontal position data	MCKF	Master clock, inverted phase	PM0-PM2	Pull-up resistors
HSCRLD	Latch playfield horizontal scroll data	MCKR	Master clock	POKEY	68010 read/write control, unbuffered
		MD0-MD15	68010 "M" data bus	PR1-PR6	
		MFLP	Motion object horizontal flip parameter	R/W	

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Gauntlet Signal Name Glossary

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Gauntlet Signal Name Glossary, continued

RAM0, RAM1 68010 working RAM chip selects
 RAUD Summed right channel audio
 RCLOCK System clock
 RD0-RD15 68010 ROM data bus
 RD68K 6502 read 68010 output buffer
 RED Red analog video output
 RED0-RED3 Red color RAM data
 RIGHT-1- RIGHT-4 Joystick right switch inputs, players 1-4
 ROM 68010 ROM data bus enable
 ROM0-ROM4 68010 program ROM chip selects
 ROMH/L 68010 program ROM high/low select (A14 on a 27256)
 ROUT0-ROUT3 Red latched digital video output
 SA0-SA15 6502 address bus unbuffered
 SBA0-SBA13 6502 buffered address bus
 SBD0-SBD7 6502 buffered data bus
 SBR/W 6502 buffered read/write control
 SBW/R 6502 buffered read/write control inverted
 SD0-SD7 6502 data bus unbuffered
 SELFTEST Self-test switch input test pad
 SID Serial input data
 SIORD 6502 miscellaneous input read control
 SIOWR 6502 output latch control
 SIRQACK 6502 interrupt acknowledge
 SLAPSTK SLAPSTIC chip select
 SM0-SM2 Speech audio mix control bits

SNDBUF 6502 output buffer full (to 68010)
 SNDINT 68010 interrupt from 6502
 SNDIRQ 6502 4-millisecond interrupt
 SNDNMI 6502 non-maskable interrupt
 SNDRD 68010 read buffer from 6502
 SNDRES 6502 master reset (controlled by 68010)
 SNDWR 68010 write to output buffer (to 6502)
 SOD Serial output data
 SPHRDY Speech chip ready
 SPHRES Speech chip reset
 SPHWR Speech chip write
 SQUEAK Speech chip operating frequency control
 SRD 6502 read phase
 START-1-START-4 Start switch inputs, players 1-4
 STEST Self-test switch input
 SWR 6502 write phase
 SYSRES System reset (power up)
 UDS 68010 upper data strobe
 UNLOCK EEPROM write enable control
 UP-1-UP-4 Joystick up switch inputs, players 1-4
 VAS0, VAS1 Video RAM address control
 (VAS0*), (VAS1*) VAS0 and VAS1 before being latched
 VBD0-VBD15 Video RAM buffered data bus
 VBKACK Vertical blank interrupt acknowledge
 VBKINT Vertical blank interrupt
 VBLANK Vertical blank

VBUS 68010 "V" bus enable (for video RAM)
 VCC System V_{cc} (5 volts regulated)
 VCPU 68010-to-video-RAM synchronization control
 VERT Latch motion object vertical data and size data
 VERTDL, VERTDL Delayed one clock cycle
 VIDBLANK Video blank (horizontal and vertical blank mixed)
 VMATCH Motion object vertical parameter matches current playfield vertical position
 VOICE Speech chip select
 VPOS0-VPOS8 Motion object vertical position data
 VRA0-VRA11 Video RAM address bus
 VRAM 68010 address decode for video RAM
 VRAMRD 68010 read from video RAM
 VRAMWE 68010 write to video RAM
 VRD0-VRD15 Video RAM data bus, unbuffered
 VRDTACK Video RAM to 68010 data acknowledge
 VSIZ0-VSIZ2 Motion object vertical size parameter
 VSYNC, VSYNC Vertical sync
 WDOG Watchdog control
 WH 68010 write high byte
 WL 68010 write low byte
 WR68K 6502 write to output buffer (to 68010)
 YAMRES Music chip reset
 YM0-YM2 Music audio mix control bits
 ZREF Intensity reference for video output

Gauntlet Signal Name Glossary, continued

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Gauntlet™ Signal
Name Glossary, Continued

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